CELLULAR

TOBY-L4 series

LTE Advanced (Cat 6) modules with 3G and 2G fallback

Data Sheet

Abstract

Technical data sheet describing TOBY-L4 series cellular modules.
The modules are a complete and cost efficient LTE-FDD, LTE-TDD, DC-HSPA+, (E)GPRS multi-mode and multi-band solution with uCPU embedded Linux programming capability. The modules offer up to 301.5 Mb/s download and up to 51.0 Mb/s upload data rates with Category 6 LTE-Advanced carrier aggregation technology in the compact TOBY form factor.

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Initial Production	Early Prod. Information	Data from product verification. Revised and supplementary data may be published later.
Mass Production / End of Life	Production Information	Final product specification.

This document applies to the following products:

Name	Type number	Modem version	Application version	PCN reference	Product Status
TOBY-L4006	TOBY-L4006-00A-00	TBD	TBD	TBD	Functional Sample
	TOBY-L4006-50A-00	40.14	A00.01	UBX-17047934	Prototype
TOBY-L4106	TOBY-L4106-00A-00	TBD	TBD	TBD	Functional Sample
	TOBY-L4106-50A-00	40.14	A00.01	UBX-17047934	Prototype
TOBY-L4206	TOBY-L4206-00A-00	TBD	TBD	TBD	Functional Sample
	TOBY-L4206-50A-00	TBD	TBD	TBD	Functional Sample
TOBY-L4906	TOBY-L4906-00A-00	TBD	TBD	TBD	Functional Sample
	TOBY-L4906-50A-00	40.19	A00.02	UBX-17058711	Engineering Sample

Contents

1 Functional description

1.1 Overview

The TOBY-L4 series modules support multi-band LTE-FDD, LTE-TDD, DC-HSPA+ and (E)GPRS radio access technologies (see Table 1) in the very small TOBY 248-pin LGA form factor (35.6 x 24.8 mm), which is easy to integrate in compact designs.

TOBY-L4 series modules are form factor compatible with the other u-blox cellular module families (including SARA, LISA, LARA, and TOBY form factors): this allows customers to take the maximum advantage of their hardware and software investments, and provides very short time-to-market.

With LTE-Advanced carrier aggregation category 6 data rates up to 301.5 Mb/s (downlink) / 51.0 Mb/s (uplink), the modules are ideal for applications requiring the highest data-rates and high-speed internet access. Reduced cost variants supporting LTE Cat 4 or LTE Cat 1 will be available for lower speed or "pure" telematics devices.

TOBY-L4 series include the following LTE Cat 6 modules with 3G and 2G fallback:

- TOBY-L4006 modules, mainly designed for operation in North America
- TOBY-L4106 modules, mainly designed for operation in Europe
- TOBY-L4206 modules, mainly designed for operation in Asia-Pacific and South America
- TOBY-L4906 modules, mainly designed for operation in China

TOBY-L4 series modules include the following product versions:

- The "00" product versions, integrating the u-blox uCPU on-chip processor to allow customers to run their dedicated applications on an embedded Linux distribution based on Yocto, with RIL-Core connectivity APIs
- The "50" product versions, which can be controlled by an external application processor through standard and u-blox proprietary AT commands described in the u-blox AT Commands Manual [1]

TOBY-L4 series modules are the ideal product for the development of all kinds of automotive devices, such as smart antennas and in-dash telematics / infotainment devices, supporting a comprehensive set of HW interfaces (including RGMII/RMII for Ethernet and analog audio) over a very extended temperature range that allow the establishment of an emergency call up to +95 °C, complemented by a set of state-of-the art security features.

TOBY-L4 series modules are also the perfect choice for consumer fixed-wireless terminals, mobile routers and gateways, applications requiring video streaming and many other industrial (M2M) applications.

TOBY-L4 series modules are manufactured in ISO/TS 16949 certified sites, with the highest production standards and the highest quality and reliability. Each module is fully tested and inspected during production. Modules are qualified according to automotive requirements as for systems installed in vehicles.

1.2 Product features

Model	Region	Bands				Interfaces													Features										Grade		
		LTE FDD bands	LTE TDD bands	UMTS FDD bands	GSM bands	UART	USB 2.0 device/host*	USB 3.0 device**	SPI	RGMII / RMII	eMMC	SDIO	DDC (I^2C)	SIM	GPIO	ADC	Antenna supervisor	CA / MIMO / Rx Diversity	Analog audio	Digital Audio	uCPU for customer applications	GNSS via modem	Wi-Fi via modem	Network indication	Jamming detection	Embedded TCP/UDP stack	Embedded HTTP, FTP, SSL	FOTA	Dual stack IPv4/IPv6	Standard	Professional	Automotive
TOBY-L4006-00	North America	2,4,5 7,12 13,29		2 4,5	850 1900	4	1	1	2	1	1	1	2	2	14	2	•	•	•	•	•	•	•	•	•	•	•	•	•			
TOBY-L4006-50	North America	2,4,5 7,12 13,29		2 4,5	850 1900		1	1						2	9		•	•	•	•					•			•	•			
TOBY-L4106-00	EMEA	1,3 7,8 20	38	1,8	900 1800	4	1	1	2	1	1	1	2	2	14	2	•	•	•	•	•	•	•	•	•	•	•	•	•			
TOBY-L4106-50	EMEA	1,3 7,8 20	38	1,8	900 1800		1	1						2	9		•	•	•	•					•			•	•			
TOBY-L4206-00	APAC, South America	1,3,5 7,8,9 19,28		1 5,8	Quad	4	1	1	2	1	1	1	2	2	14	2	•	•	•	•	•	•	•	•	•	•	•	•	•			
TOBY-L4206-50	APAC, South America	1,3,5 7,8,9 19,28		1 5,8	Quad		1	1						2	9		•	•	•	•					•			•	•			
TOBY-L4906-00	China	1,3	39 40,41	1,8	900 1800	4	1	1	2	1	1	1	2	2	14	2	•	•	•	•	•	•	•	•	•	•	•	•	•			
TOBY-L4906-50	China	1,3	39 40,41	1,8	900 1800		1	1						2	9		•	•	•	•					•			•	•			

* USB 2.0 host role not supported by "50" product versions

** USB 3.0 interface supported by future firmware versions

Table 1: TOBY-L4 series main features summary

1.3 Block diagram

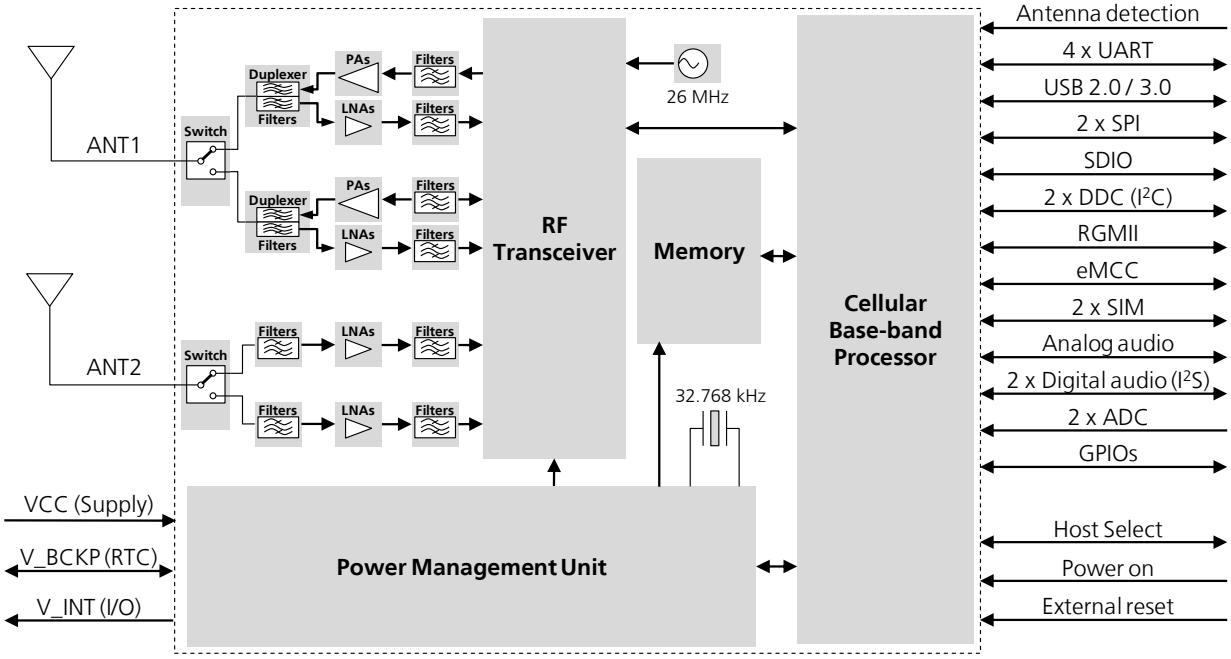


Figure 1: TOBY-L4 series block diagram

TOBY-L4 series modules "00" product versions do not support the following interfaces, which should be left unconnected and should not be driven by external devices:

- USB 3.0 interface
- Second digital audio interface (I2S1)

TOBY-L4 series modules "50" product versions do not support the following interfaces, which should be left unconnected and should not be driven by external devices:

- USB 3.0 interface
- UART interfaces
- SPI interfaces
- SDIO interface
- DDC (I^2C) interfaces
- RGMII / RMII interface
- eMMC interface
- Second digital audio interface (I2S1)
- ADC pins
- Host Select pins

1.4 Product description

TOBY-L4 series modules provide multi-band 4G / 3G / 2G multi-mode radio access technologies, based on the 3GPP Release 10 protocol stack, with the main characteristics summarized in Table 2 and Table 3.

LTE	3G	2G
LTE-Advanced Carrier Aggregation Frequency Division Duplex (LTE FDD) Time Division Duplex (LTE TDD) Down-Link CA / MIMO / Rx diversity	Dual-Cell High Speed Packet Access Frequency Division Duplex (UMTS FDD) Down-Link Rx diversity	Enhanced Data rate GSM Evolution (EDGE) Time Division Multiple Access (TDMA) DL Advanced Rx Performance Phase 1
LTE FDD Power Class • Class 3 (23 dBm) LTE TDD Power Class • Class 3 (23 dBm)	UMTS FDD Power Class • Class 3 (24 dBm)	GMSK Power Class • Class 4 (33 dBm) for GSM/E-GSM bands • Class 1 (30 dBm) for DCS/PCS bands 8-PSK Power Class • Class E2 (27 dBm) for GSM/E-GSM bands • Class E2 (26 dBm) for DCS/PCS bands

Data rate
• LTE category 6:
  • up to 301.5 Mb/s DL
  • up to 51.0 Mb/s UL
	Data rate
	• FDD UE categories:
	  • DL cat.24, up to 42.2 Mb/s
	  • UL cat.6, up to 5.76 Mb/s
		Data rate
		• GPRS multi-slot class 33, CS1-CS4:
		  • up to 107.0 kbit/s DL
		  • up to 85.6 kbit/s UL
		• EDGE multi-slot class 33, MCS1-MCS9
		  • up to 296.0 kbit/s DL
		  • up to 236.8 kbit/s UL

Table 2: TOBY-L4 series LTE, 3G and 2G main characteristics summary

Module	Region	LTE FDD bands	LTE TDD bands	LTE CA	UMTS FDD bands	GSM bands
TOBY-L4006	North America	12 (700 MHz) 17 (700 MHz) 29 (700 MHz) 13 (750 MHz) 5 (850 MHz) 4 (1700 MHz) 2 (1900 MHz) 7 (2600 MHz)		4 + 17 2 + 13 2 + 17 2 + 29 4 + 5 4 + 4 4 + 13 4 + 29	5 (850 MHz) 4 (1700 MHz) 2 (1900 MHz)	GSM 850 PCS 1900
TOBY-L4106	EMEA, APAC	20 (800 MHz) 8 (900 MHz) 3 (1800 MHz) 1 (2100 MHz) 7 (2600 MHz)	38 (2600 MHz)	3 + 20 7 + 20 3 + 3 3 + 7	8 (900 MHz) 1 (2100 MHz)	E-GSM 900 DCS 1800
TOBY-L4206	APAC, South America	28 (750 MHz) 19 (850 MHz) 5 (850 MHz) 8 (900 MHz) 9 (1800 MHz) 3 (1800 MHz) 1 (2100 MHz) 7 (2600 MHz)		3 + 28 3 + 7 7 + 28 3 + 3 1 + 8 3 + 19 1 + 19	5 (850 MHz) 8 (900 MHz) 1 (2100 MHz)	GSM 850 E-GSM 900 DCS 1800 PCS 1900
TOBY-L4906	China	3 (1800 MHz) 1 (2100 MHz)	39 (1900 MHz) 40 (2300 MHz) 41 (2500 MHz)	3 + 3 40 + 40 41 + 41 39 + 41	8 (900 MHz)[1] 1 (2100 MHz)	E-GSM 900 DCS 1800

Table 3: TOBY-L4 series supported Bands and Carrier Aggregation combinations summary

[1] Down-Link Rx diversity not supported on this band

1.5 AT command support

AT commands are not supported by the "00" product versions.

The TOBY-L4 series modules "50" product versions support the standard AT commands according to the 3GPP specifications TS 27.007 [7], TS 27.005 [8], and u-blox proprietary AT commands.

For the complete list of all supported AT commands and their syntax, see the u-blox AT Commands Manual [1].

1.6 u-blox uCPU on-chip processor for OEM applications

The u-blox uCPU on-chip processor for OEM applications is not supported by "50" product versions.

The TOBY-L4 series modules "00" product versions integrate the u-blox uCPU on-chip processor, based on a powerful quad-core CPU, to allow customers to run their dedicated applications on an embedded Linux distribution based on Yocto, with RIL-Core connectivity APIs.

The Hardware Virtual Machine Manager is implemented for low latency, fault tolerance, security and protection, providing hardware virtualization between the modem and application systems, including a dedicated virtual machine for security management (see Figure 2).

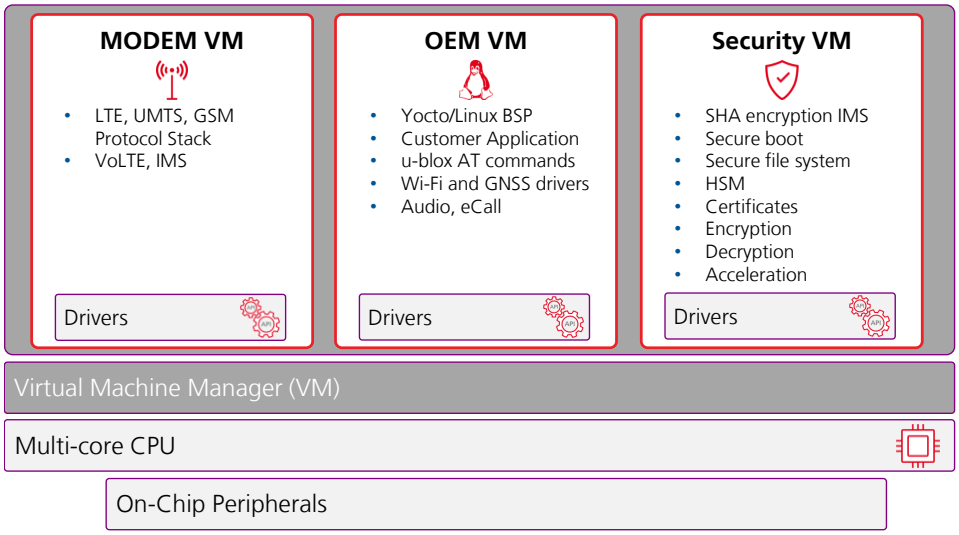


Figure 2: TOBY-L4 series SW architecture

Full separation between the modem, security and application virtual machines is implemented, with the latest Yocto available for customers with full access to the HW and Kernel (Yocto BSP).

Advanced security implementation is available, with

- Secure boot and secure update
- Crypto HW accelerator / true random number generator
- Secure debugging
- Secure file system
- Secure services provided by dedicated security Virtual Machine / trusted execution environment

For more details regarding the u-blox uCPU architecture and OEM applications development, see the TOBY-L4 SDK Application Note [3], the TOBY-L4 uCPU Build System Application Note [4], and the TOBY-L4 uCPU Platform Software Architecture Application Note [5].

2 Interfaces

2.1 Power management

2.1.1 Module supply input (VCC)

TOBY-L4 series modules must be supplied through the **VCC** pins by a DC power supply. Voltage must be stable, because the current drawn from **VCC** can vary significantly during operation, based on the power consumption profile of the LTE/3G/2G technologies (described in the TOBY-L4 series System Integration Manual [2]).

2.1.2 RTC supply input / output (V_BCKP)

When the **VCC** voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the Real Time Clock (RTC) through the rail available at the **V_BCKP** pin. If the **VCC** voltage is under the minimum operating limit (e.g. during not powered mode), the RTC can be externally supplied through the **V_BCKP** pin.

2.1.3 Generic digital interfaces supply output (V_INT)

TOBY-L4 series modules provide a 1.8 V supply rail output on the **V_INT** pin, which is internally generated when the module is switched on. The same voltage domain is used internally to supply the generic digital interfaces of the modules. The **V_INT** supply output can be used in place of an external discrete regulator.

2.2 Antenna interfaces

2.2.1 Antenna RF interfaces

The modules have two RF pins with a characteristic impedance of 50 Ω. The primary antenna pin (**ANT1**) supports both Tx and Rx, providing the main antenna interface, while the secondary antenna pin (**ANT2**) supports Rx only for Carrier Aggregation (CA), Multiple-Input Multiple Output (MIMO) and Rx diversity.

2.2.2 Antenna detection

The **ANT_DET** pin is an Analog to Digital Converter (ADC) input with a current source provided by the TOBY-L4 modules to sense the antenna presence (as an optional feature). It evaluates the resistance from the **ANT1** and **ANT2** pins to GND by means of an external antenna detection circuit implemented on the application board. For more details, see the TOBY-L4 series System Integration Manual [2].

2.3 System functions

2.3.1 Module power-on

TOBY-L4 series can be switched on in the following way:

- Low pulse on the **PWR_ON** pin, which is normally set high by an internal pull-up, for a valid time period when the applied **VCC** voltage is within the valid operating range (see section 4.2.8). The **PWR_ON** line should be driven by an open drain, open collector or contact switch.

2.3.2 Module power-off

TOBY-L4 series can be properly switched off, saving current parameter settings in the module's non-volatile memory and performing a proper network detach, by:

- AT+CPWROFF command[2] (see the u-blox AT Commands Manual [1])
- uCPU application[3]
- Low pulse on the **PWR_ON** pin, which is normally set high by an internal pull-up, for a valid time period (see section 4.2.8, module normal switch-off). The current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

An abrupt under-voltage shutdown occurs on TOBY-L4 series modules when the **VCC** supply is removed. If this occurs, it is not possible to store the current parameter settings in the module's non-volatile memory or to perform the proper network detach.

An abrupt emergency shutdown occurs on TOBY-L4 series modules when a sufficiently long low pulse is set at the **PWR_ON** pin (see section 4.2.8, module emergency switch-off). In this case, storage of the current parameter settings in the module's non-volatile memory and a proper network detach are not performed.

An over-temperature shutdown occurs on TOBY-L4 modules when the temperature measured within the cellular module reaches a critical range. For more details, see the TOBY-L4 series System Integration Manual [2].

2.3.3 Module reset

TOBY-L4 series modules can be properly reset (rebooted), performing an "internal" or "software" reset of the module, saving current parameter settings in the module's non-volatile memory and performing a proper network detach, by:

- AT+CFUN command[2] (see the u-blox AT Commands Manual [1])
- uCPU application[3]

An abrupt "external" or "hardware" reset occurs when a low level is applied to the **RESET_N** pin, which is normally set high by an internal pull-up, for a valid time period (see the section 4.2.9). The current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed. The **RESET_N** line should be driven by an open drain, open collector or contact switch.

2.3.4 Module configuration selection by host processor

☞ Host Select pins are not supported by the "50" product version.

TOBY-L4 series modules include two 1.8 V digital pins (**HOST_SELECT0**, **HOST_SELECT1**), which can be configured for External Interrupt detection or as GPIO by means of uCPU application.

[2] Not supported by "00" product version
[3] Not supported by "50" product version

2.4 SIM

2.4.1 SIM interfaces

TOBY-L4 series modules provide two SIM interfaces for the direct connection of two external SIM cards/chips, which can be alternatively used (only one SIM at a time can be used for network access):

- SIM0 interface (**VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST** pins), which is enabled by default
- SIM1 interface (**VSIM1**, **SIM1_IO**, **SIM1_CLK**, **SIM1_RST** pins), which can be alternatively enabled by dedicated AT command[4] (see the u-blox AT Commands Manual [1]), or by means of uCPU application[5].

Both 1.8 V and 3 V SIM types are supported. Activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The high-speed SIM/ME interface and PPS procedure for baud rate selection are implemented according to the values proposed by the SIM card/chip.

2.4.2 SIM detection

TOBY-L4 series modules provide the SIM detection function over GPIO to detect the mechanical / physical presence of an external SIM card connected to the SIM0 interface (as an optional feature) when the specific GPIO of the module is properly connected to the mechanical switch of the SIM card holder (for more details, see the TOBY-L4 series System Integration Manual [2]).

2.5 Serial communication

TOBY-L4 series provides the following serial communication interfaces:

- USB interface: USB Super-Speed 3.0 compliant interface[6] and USB High-Speed 2.0 compliant interface available for communication with an external host application processor or device[7]
- Up to four UART interfaces[8]: Universal Asynchronous Receiver/Transmitter serial interfaces available for communication with an external host application processor and/or other serial devices
- Up to two SPI interfaces[5]: Serial Peripheral Interfaces available for communication with external SPI devices
- Two DDC interfaces[5]: I^2C bus compatible interfaces available for communication with external u-blox GNSS positioning chips and modules, and/or other I^2C devices as an audio codec
- SDIO interface[5]: Secure Digital Input Output interface available for communication with external u-blox short range radio communication Wi-Fi / Bluetooth modules, or other SDIO devices
- RGMII interface[5]: Reduced Gigabit Media-Independent Interface, where the module represents an Ethernet MAC, which can be connected to an external Ethernet PHY for communication with a remote processor

[4] Not supported by "00" product version
[5] Not supported by "50" product version
[6] USB 3.0 interface will be supported by future firmware versions
[7] USB 2.0 host role is not supported by "50" product versions
[8] UART interfaces are not supported by "50" product version, except for diagnostic purpose and Ring Indicator function over UART0

2.5.1 USB interface

☞ USB Super-Speed 3.0 compliant interface will be supported by future firmware version.

☞ USB High-Speed 2.0 host role is not supported by "50" product versions.

TOBY-L4 series modules include a USB Super-Speed 3.0 compliant interface, supporting up to 5 Gb/s data rate, and also including a USB High-Speed 2.0 compliant interface, supporting up to 480 Mb/s data rate.

The USB High-Speed 2.0 compliant interface consists of the following pins:

- **USB_D+/USB_D–**, USB High-Speed differential transceiver data lines as per USB 2.0 specification [14]
- **VUSB_DET** input pin, which senses the VBUS USB supply presence (nominally 5 V at the source) to detect the host connection and enable the USB 2.0 interface with the module acting as USB device.

  Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input pin, which senses the VBUS USB supply voltage presence and absorbs only a few microamperes.
- **USB_ID** pin, available for USB ID resistance measurement:
  - if the **USB_ID** pin is externally connected to GND, then the module acts as a USB host
  - if the **USB_ID** pin is externally left unconnected (floating), than the module acts as a USB device

The USB High-Speed 2.0 compliant interface, with the module acting as a USB device, provides:

- AT commands[9]
- Data communication
- Ethernet-over-USB virtual channel
- Auxiliary channel for audio tuning
- Trace log capture (diagnostic purpose)
- Linux console for uCPU applications development and debug[10]
- FW upgrades by means of the u-blox EasyFlash tool and/or by means of the FOAT[9] feature

The USB High-Speed 2.0 compliant interface, with the module acting as USB host (OTG), provides:

- Communication with external device by means of uCPU application

The USB Super-Speed 3.0 compliant interface as per the USB 3.0 specification [13], with the module acting as a USB device, consists of the following additional pins:

- **USB_SSTX+/USB_SSTX–**, USB Super-Speed differential transmitter data lines
- **USB_SSRX+/USB_SSRX–**, USB Super-Speed differential receiver data lines

USB drivers are available for Windows operating system platforms. TOBY-L4 series modules are compatible with standard Linux/Android USB kernel drivers.

[9] Not supported by "00" product version
[10] Not supported by "50" product version

2.5.2 UART interfaces

☞ UART interfaces are not supported by the "50" product version, except for trace logging (diagnostic purposes) and Ring Indicator functionality over the UART0 interface.

2.5.2.1 UART0 interface

The UART0 Universal Asynchronous Receiver/Transmitter serial interface has CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), providing:

- Communication with external devices by means of the uCPU API, over the following pins:
  - **RXD** module output and **TXD** module input data lines
  - **CTS** module output and **RTS** module input hardware flow control lines
- Trace logging (diagnostic purpose), over the following pins:
  - **RXD** module output and **TXD** module input data lines
- Ring Indicator functionality, over the following pin:
  - **RI** module output line

The UART0 interface can operate at 9.6 kbit/s, 19.2 kbit/s, 38.4 kbit/s, 57.6 kbit/s, 115.2 kbit/s, 230.4 kbit/s, 460.8 kbit/s, 921.6 kbit/s, 3 Mbit/s, 3.25 Mbit/s and 6.5 Mbit/s baud rates, with 8N1 frame format, and with hardware flow control output (**CTS** line) driven to OFF state when the module is not prepared to accept data by the UART0 interface.

The **DTR**, **DSR**, **DCD** and **RI** pins can be alternatively configured for External Interrupt detection or as GPIO by means of the uCPU API. The **RI** pin can be alternatively configured as GPIO by AT command.

For more details see the TOBY-L4 series System Integration Manual [2], and the u-blox AT Commands Manual [1] +CNMI, +URING AT commands.

2.5.2.2 UART1 interface

The UART1 Universal Asynchronous Receiver/Transmitter serial interface has CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), providing:

- Communication with external devices by means of uCPU API, over the following pins:
  - **RXD1** module output and **TXD1** module input data lines
  - **CTS1** module output and **RTS1** module input hardware flow control lines

The UART1 interface can operate at 9.6 kbit/s, 19.2 kbit/s, 38.4 kbit/s, 57.6 kbit/s, 115.2 kbit/s, 230.4 kbit/s, 460.8 kbit/s, 921.6 kbit/s, 3 Mbit/s, 3.25 Mbit/s and 6.5 Mbit/s baud rates, with 8N1 frame format, and with hardware flow control output (**CTS1** line) driven to OFF state when the module is not prepared to accept data by the UART1 interface.

The UART1 interface can be alternatively, in mutually exclusive way, configured as SPI1 interface by means of uCPU API, for communication with external devices with the following pins:

- **RXD1** pin, alternatively configured as SPI1 Master Output Slave Input (module output)
- **TXD1** pin, alternatively configured as SPI1 Master Input Slave Output (module input)
- **CTS1** pin, alternatively configured as SPI1 Chip Select (module output)
- **RTS1** pin, alternatively configured as SPI1 Clock (module output)

2.5.2.3 UART2 interface

The UART2 Universal Asynchronous Receiver/Transmitter serial interface has CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), providing:

- Communication with external devices by means of uCPU API, over the following pins:
  - **RXD2** module output and **TXD2** module input data lines

The UART2 interface can operate at 9.6 kbit/s, 19.2 kbit/s, 38.4 kbit/s, 57.6 kbit/s, 115.2 kbit/s, 230.4 kbit/s, 460.8 kbit/s, 921.6 kbit/s, 3 Mbit/s, 3.25 Mbit/s and 6.5 Mbit/s baud rates, with 8N1 frame format.

2.5.2.4 UART3 interface

The UART3 Universal Asynchronous Receiver/Transmitter serial interface has CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), providing:

- Linux console for uCPU API development and debug, over the following pins:
  - **RXD3** module output and **TXD3** module input data lines

The UART3 interface can operate at 9.6 kbit/s, 19.2 kbit/s, 38.4 kbit/s, 57.6 kbit/s, 115.2 kbit/s, 230.4 kbit/s, 460.8 kbit/s, 921.6 kbit/s, 3 Mbit/s, 3.25 Mbit/s and 6.5 Mbit/s baud rates, with 8N1 frame format.

2.5.3 SPI interfaces

☞ SPI interfaces are not supported by "50" product version.

2.5.3.1 SPI0 interface

The SPI0 1.8 V Serial Peripheral Interface supports communication with an external SPI slave devices, with the module acting as SPI master, by means of uCPU API, with the following pins:

- **SPI_MOSI** pin, SPI0 Master Output Slave Input (module output)
- **SPI_MISO** pin, SPI0 Master Input Slave Output (module input)
- **SPI_SCLK** pin, SPI0 Serial Clock (module output)
- **SPI_CS** pin, SPI0 Chip Select 0 (module output)
- **GPIO4** pin, alternatively configured as SPI0 Chip Select 1 (module output)

The SPI0 Serial Clock signal can be configured to different operating frequencies: 26 MHz (maximum frequency), and 26 / n MHz, where n is 2, 3, 4, etc.

For more details regarding the SPI0 interface usage and the integration with an external application processor and/or other SPI devices, see the TOBY-L4 series System Integration Manual [2].

2.5.3.2 SPI1 interface

The SPI1 1.8 V Serial Peripheral Interface supports communication with an external SPI slave devices, with the module acting as SPI master, by means of the uCPU API, with the following UART1 pins configured as alternative functions, in a mutually exclusive way:

- **RXD1** pin, alternatively configured as SPI1 Master Output Slave Input (module output)
- **TXD1** pin, alternatively configured as SPI1 Master Input Slave Output (module input)
- **RTS1** pin, alternatively configured as SPI1 Serial Clock (module output)
- **CTS1** pin, alternatively configured as SPI1 Chip Select (module output)

The SPI1 Serial Clock signal can be configured to various operating frequencies: 26 MHz (maximum frequency), and (26 / n) MHz, where n is 2, 3, 4, etc.

For more details regarding the SPI1 interface usage and the integration with an external application processor and/or other SPI devices, see the TOBY-L4 series System Integration Manual [2].

2.5.4 DDC (I²C) interfaces

☞ DDC (I²C) interfaces are not supported by the "50" product version.

2.5.4.1 I2C0 interface

The **SDA** and **SCL** pins represent the I2C0 1.8 V I²C bus compatible Display Data Channel (DDC) interface, with the module acting as I²C master, available for

- communication with u-blox GNSS chips / modules
- communication with other external I²C devices by means of uCPU API

The I2C0 interface pins of the module are open drain outputs conforming to the I²C bus specifications [15], supporting up to 100 kbit/s data rate in Standard-mode, and up to 400 kbit/s data rate in Fast-mode. External pull up resistors to a suitable 1.8 V supply (e.g. **V_INT**) are required for operations.

For more details regarding the I2C0 interface usage and the integration with a u-blox GNSS receiver, see the TOBY-L4 series System Integration Manual [2].

2.5.4.2 I2C1 interface

The **SDA** and **SCL** pins represent the I2C1 I²C bus compatible Display Data Channel (DDC) interface, with the module acting as I²C master, available for

- communication with other external I²C devices by means of uCPU API

The I2C1 interface pins of the module are open drain outputs conforming to the I²C bus specifications [15], supporting up to 100 kbit/s data rate in Standard-mode, and up to 400 kbit/s data rate in Fast-mode. External pull up resistors to a suitable 1.8 V supply (e.g. **V_INT**) are required for operations.

For more details regarding the I2C1 interface usage, see the TOBY-L4 series System Integration Manual [2].

2.5.5 SDIO interface

☞ SDIO interface is not supported by the "50" product version.

TOBY-L4 series modules include a 4-bit Secure Digital Input Output interface (**SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK**, **SDIO_CMD**), where the module acts as an SDIO host controller designed to:

- communicate with compatible u-blox short range radio communication modules by means of the uCPU API
- communicate with external SDIO devices by means of the uCPU API

The SDIO interface supports up to 832 Mbit/s data rate with SD 3.0 SDR104 mode at 208 MHz clock frequency.

For more details regarding the SDIO interface usage, see the TOBY-L4 series System Integration Manual [2].

2.5.6 RGMII interface

☞ RGMII interface is not supported by the "50" product version.

TOBY-L4 series modules include an Ethernet Media Access Control (MAC) block supporting up to 1 Gbit/s data rate via a Reduced Gigabit Media-Independent Interface compliant with the RGMII Version 1.3 specification [16] and the RMII Revision 1.2 specification [17].

The module represents an Ethernet MAC controller, which can be connected to an external Ethernet physical transceiver (PHY) chip for communication with a remote processor over Ethernet.

The following signals are provided for communication and management of an external Ethernet PHY:

- **V_ETH** Interface supply output
- **ETH_TX_CLK** RGMII Transmit reference Clock (TXC) output
  RMII Reference Clock (REF_CLK) output
- **ETH_TX_CTL** RGMII Transmit Control output, driven on both edges of the Transmit clock (TXC)
  RMII Transmit Enable (TXEN) output, synchronous with Reference Clock (REF_CLK)
- **ETH_TXD0** RGMII / RMII Transmit Data [0], from MAC to PHY (module output)
- **ETH_TXD1** RGMII / RMII Transmit Data [1], from MAC to PHY (module output)
- **ETH_TXD2** RGMII Transmit Data [2], from MAC to PHY (module output)
- **ETH_TXD3** RGMII Transmit Data [3], from MAC to PHY (module output)
- **ETH_RX_CLK** RGMII Receive reference Clock (RXC) input
- **ETH_RX_CTL** RGMII Receive Control input, sampled on both edges of the Receive clock (RXC)
  RMII Carrier Sense (CRS) / Receive Data Valid (RX_DV) input
- **ETH_RXD0** RGMII / RMII Receive Data [0], from PHY to MAC (module input)
- **ETH_RXD1** RGMII / RMII Receive Data [1], from PHY to MAC (module input)
- **ETH_RXD2** RGMII Receive Data [2], from PHY to MAC (module input)
- **ETH_RXD3** RGMII Receive Data [3], from PHY to MAC (module input)
- **ETH_INTR** Ethernet Interrupt Input, from PHY to MAC (module input)
  When this signal is high, it indicates an interrupt event in the PHY
- **ETH_MDIO** Management Data Input Output, bidirectional signal (module input/output)
- **ETH_MDC** Management Data Clock, from MAC to PHY (module output)

For more details regarding the RGMII interface usage and its integration, see the TOBY-L4 series System Integration Manual [2].

2.6 eMMC interface

☞ eMMC interface is not supported by the "50" product version.

TOBY-L4 series modules include a 4-bit embedded Multi-Media Card interface compliant with the JESD84-B451 Embedded Multimedia Card (eMMC) Electrical Standard 4.51 [18]. The following signals are provided for connection and management of an external eMMC / SD memory, by means of the uCPU API:

- **V_MMC** Interface supply output (module output)
- **MMC_D0** Multi-Media Card Data [0], bidirectional signal (module input/output)
- **MMC_D1** Multi-Media Card Data [1], bidirectional signal (module input/output)
- **MMC_D2** Multi-Media Card Data [2], bidirectional signal (module input/output)
- **MMC_D3** Multi-Media Card Data [3], bidirectional signal (module input/output)
- **MMC_CMD** Multi-Media Card Command, bidirectional signal (module input/output)
- **MMC_CLK** Multi-Media Card Clock (module output)
- **MMC_RST_N** Multi-Media Card Reset (module output)
- **MMC_CD_N** Multi-Media Card Detect (module input)

For more details regarding the eMMC interface usage and the integration with an external memory, see the TOBY-L4 series System Integration Manual [2].

2.7 Audio interfaces

TOBY-L4 series modules provide analog and digital audio interfaces:

- Analog audio inputs:
  - First differential analog audio input (**MIC1_P**, **MIC1_N**), which can be connected to the output of an external analog audio device, or an external microphone
  - Second differential analog audio input (**MIC2_P**, **MIC2_N**), which can be connected to the output of an external analog audio device, or an external microphone
  - Supply output for external microphones (**MIC_BIAS**), which can provide the bias / supply for external microphones by means of a simple circuit implemented on the application board
  - Local ground for the external microphone (**MIC_GND**), internally connected to ground as a sense line, representing a clean ground reference for the analog audio input
- Analog audio output:
  - Differential analog audio output (**SPK_P**, **SPK_N**), which can be connected to the input of an external analog audio device, or an external speaker
- Digital audio interfaces:
  - I2S0 digital audio interface (**I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**)

    Digital audio interface configurable in PCM mode (short synchronization signal) or in normal I²S mode (long synchronization signal) to transfer digital audio data with an external digital audio device
  - I2S1 digital audio interface[11] (**I2S1_TXD**, **I2S1_RXD**, **I2S1_CLK**, **I2S1_WA**)

    Digital audio interface configurable in PCM mode (short synchronization signal) or in normal I²S mode (long synchronization signal) to transfer digital audio data with an external digital audio device

For more details regarding the I²S digital audio interface usage and the integration with an external digital audio device as an audio codec, see the TOBY-L4 series System Integration Manual [2] and the audio AT commands description in the u-blox AT Commands Manual [1].

[11] I2S1 digital audio interface will be supported by future FW versions

2.8 ADC interfaces

☞ ADC pins are not supported by the "50" product version.

TOBY-L4 series modules include Analog to Digital Converter inputs (**ADC1**, **ADC2**), which can be handled by means of dedicated uCPU API. For more details, see the TOBY-L4 series System Integration Manual [2].

2.9 GPIO interfaces

TOBY-L4 series modules "00" product versions include 14 pins (**GPIO1**, **GPIO2**, **GPIO3**, **GPIO4**, **GPIO5**, **GPIO6**, **GPIO7**, **GPIO8**, **HOST_SELECT0**, **HOST_SELECT1**, **DTR**, **DSR**, **DCD**, and **RI**) that can be configured by the uCPU application as general purpose input/output or to provide custom functions as summarized in Table 4.

Function	Description	Configurable GPIOs
External Interrupt	External Interrupt detection (module input)	GPIO3, HOST_SELECT0-1, DTR, DSR, DCD, RI
SPI Chip Select	SPI0 Chip Select 1 (module output)	GPIO4
GNSS supply enable	Enable/disable the supply of u-blox GNSS receiver connected to the cellular module over I2C0 interface	GPIO2
GNSS data ready	Sense when u-blox GNSS receiver connected to the module is ready for sending data over I2C0 interface	GPIO3
GNSS RTC sharing	RTC synchronization signal to the u-blox GNSS receiver connected to the cellular module over I2C0 interface	GPIO4
Wi-Fi enable	Switch-on/off the external u-blox Wi-Fi module connected to the cellular module over SDIO interface	GPIO1
Input	Input to sense high or low digital level	GPIO1-8, HOST_SELECT0-1, DTR, DSR, DCD, RI
Output	Output to set the high or the low digital level	GPIO1-8, HOST_SELECT0-1, DTR, DSR, DCD, RI
Pin disabled	Output tri-stated with an internal active pull-down enabled	GPIO1-8, HOST_SELECT0-1, DTR, DSR, DCD, RI

Table 4: TOBY-L4 series modules "00" product versions GPIO custom functions summary

TOBY-L4 series modules "50" product versions include 9 pins (**GPIO1**, **GPIO2**, **GPIO3**, **GPIO4**, **GPIO5**, **GPIO6**, **GPIO7**, **GPIO8**, and **RI**) that can be configured by AT commands as general purpose input/output or to provide custom functions as summarized in Table 5.

Function	Description	Configurable GPIOs
Ring Indicator	UART0 Ring Indicator functionality (Circuit 125 in ITU-T V.24)	RI
SIM card detection	External SIM card physical presence detection	GPIO5
SIM card hot insertion/removal	Enable / disable SIM interface upon detection of external SIM card physical insertion / removal	GPIO5
Input	Input to sense high or low digital level	GPIO1-8, RI
Output	Output to set the high or the low digital level	GPIO1-8, RI
Pin disabled	Output tri-stated with an internal active pull-down enabled	GPIO1-8, RI

Table 5: TOBY-L4 series modules "50" product versions GPIO custom functions summary

3 Pin definition

3.1 Pin assignment

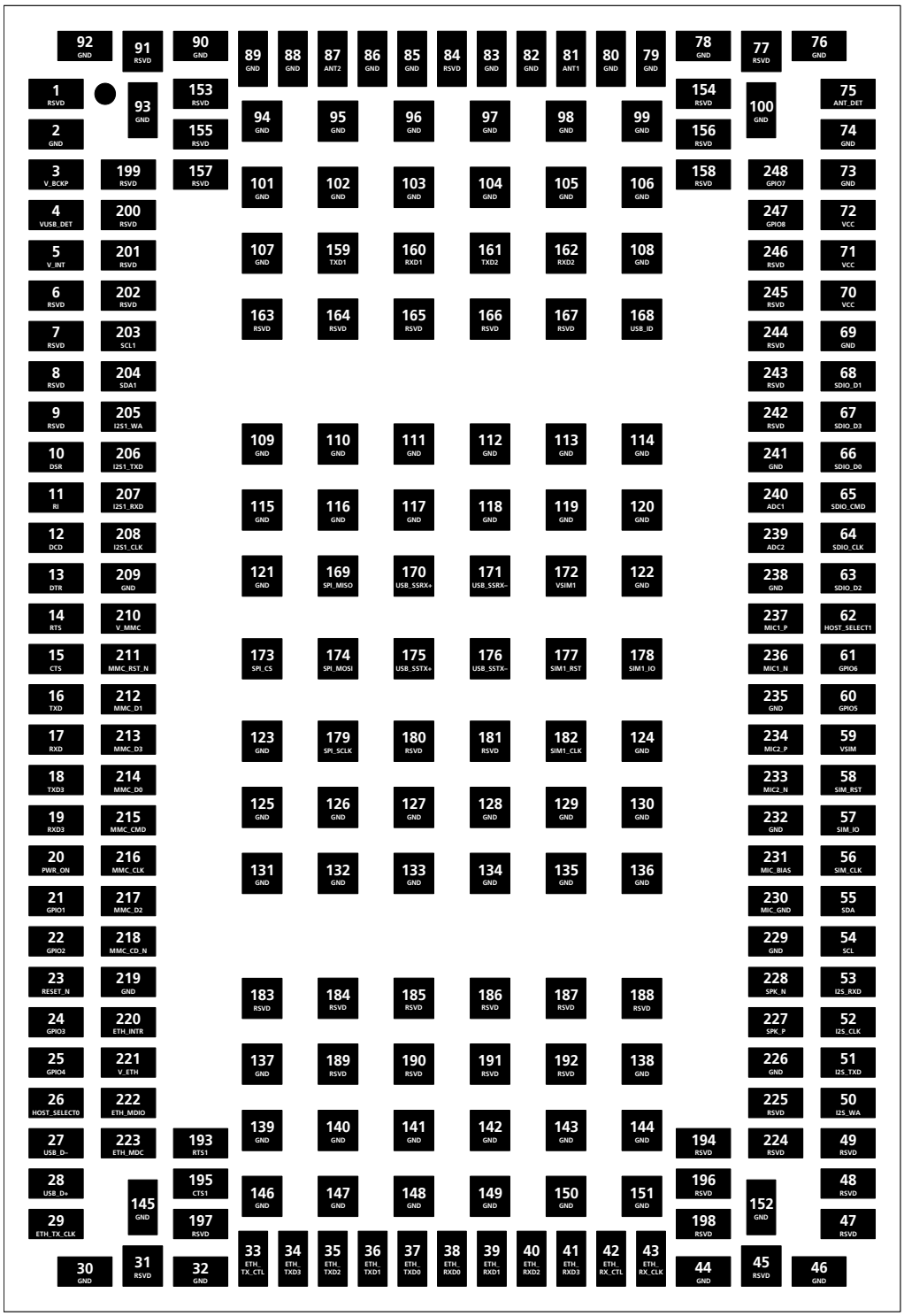


Figure 3: TOBY-L4 series pin assignment (top view: module through view)

No	Name	Power domain	I/O	Description	Remarks
1	RSVD	-	N/A	RESERVED pin	Leave unconnected.
2	GND	GND	N/A	Ground	All GND pins must be connected to ground.
3	V_BCKP	-	I/O	RTC backup supply	If the VCC module main supply input voltage is below the operating range, the RTC block can be externally supplied through the V_BCKP pin. See section 4.2.3 for detailed electrical specs.
4	VUSB_DET	USB	I	VBUS USB detect input	VBUS (5 V typical) must be connected to this pin to enable the module USB device interface. See section 4.2.11 for detailed electrical specs.
5	V_INT	GDI	O	Generic Digital Interfaces supply output	1.8 V (typical) output voltage generated by the module when it is switched-on. See section 4.2.3 for detailed electrical specs.
6	RSVD	-	N/A	RESERVED pin	This pin has special function: it must be connected to GND to allow module to work properly.
7	RSVD	-	N/A	RESERVED pin	Leave unconnected.
8	RSVD	-	N/A	RESERVED pin	Leave unconnected.
9	RSVD	-	N/A	RESERVED pin	Leave unconnected.
10	DSR	GDI	I/O / I	GPIO / External Interrupt	Alternately settable as GPIO by uCPU API Alternately settable as External Interrupt by uCPU API See section 4.2.15 for detailed electrical specs.
11	RI	GDI	O / I/O / I	UART0 ring indicator / GPIO / External Interrupt	Circuit 125 (RI) in ITU-T V.24. Alternately settable as GPIO by uCPU API / AT+UGPIOC Alternately settable as External Interrupt by uCPU API See section 4.2.15 for detailed electrical specs.
12	DCD	GDI	I/O / I	GPIO / External Interrupt	Alternately settable as GPIO by uCPU API Alternately settable as External Interrupt by uCPU API See section 4.2.15 for detailed electrical specs.
13	DTR	GDI	I/O / I	GPIO / External Interrupt	Alternately settable as GPIO by uCPU API Alternately settable as External Interrupt by uCPU API See section 4.2.15 for detailed electrical specs.
14	RTS	GDI	I	UART0 ready to send	Circuit 105 (RTS) in ITU-T V.24. See section 4.2.15 for detailed electrical specs.
15	CTS	GDI	O	UART0 clear to send	Circuit 106 (CTS) in ITU-T V.24. See section 4.2.15 for detailed electrical specs.
16	TXD	GDI	I	UART0 data input	Circuit 103 (TxD) in ITU-T V.24. See section 4.2.15 for detailed electrical specs.
17	RXD	GDI	O	UART0 data output	Circuit 104 (RxD) in ITU-T V.24. See section 4.2.15 for detailed electrical specs.
18	TXD3	GDI	I	UART3 data input	Circuit 103 (TxD) in ITU-T V.24. See section 4.2.15 for detailed electrical specs.
19	RXD3	GDI	O	UART3 data output	Circuit 104 (RxD) in ITU-T V.24. See section 4.2.15 for detailed electrical specs.
20	PWR_ON	POS	I	Power-on input	Active-low module power-on input. Internal 35 kΩ pull-up resistor to 1.3 V rail. See section 4.2.8 for detailed electrical specs.
21	GPIO1	GDI	I/O	GPIO	GPIO configurable as described in section 2.9. See section 4.2.15 for detailed electrical specs.
22	GPIO2	GDI	I/O	GPIO	GPIO configurable as described in section 2.9. See section 4.2.15 for detailed electrical specs.
23	RESET_N	ERS	I	External reset input	Active-low module reset input. Internal 100 kΩ pull-up resistor to V_INT. See section 4.2.9 for detailed electrical specs.
24	GPIO3	GDI	I/O / I	GPIO / External Interrupt	GPIO configurable as described in section 2.9. Alternately settable as External Interrupt by uCPU API See section 4.2.15 for detailed electrical specs.

No	Name	Power domain	I/O	Description	Remarks
25	GPIO4	GDI	I/O / O	GPIO / SPI0 Chip Select 1	GPIO configurable as described in section 2.9. Alternately settable as SPI0 Chip Select 1 by uCPU API. See section 4.2.15 for detailed electrical specs.
26	HOST_SELECT0	GDI	I / I/O	Input for selection of module setting by the host processor	Alternately settable as GPIO by uCPU API Alternately settable as External Interrupt by uCPU API See section 4.2.15 for detailed electrical specs.
27	USB_D–	USB2	I/O	USB High-Speed 2.0 differential transceiver (–)	90 Ω nominal differential characteristic impedance Pull-up, pull-down, series resistors as per USB 2.0 [14] are part of the pin driver: not needed externally. See section 4.2.11 for detailed electrical specs.
28	USB_D+	USB2	I/O	USB High-Speed 2.0 differential transceiver (+)	90 Ω nominal differential characteristic impedance Pull-up, pull-down, series resistors as per USB 2.0 [14] are part of the pin driver: not needed externally. See section 4.2.11 for detailed electrical specs.
29	ETH_TX_CLK	ETH	O	Ethernet Transmission Clock	RGMII: Transmit reference clock (TXC) RMII: Reference clock (REF_CLK) See section 4.2.13 for detailed electrical specs.
30	GND	GND	N/A	Ground	All GND pins must be connected to ground.
31	RSVD	-	N/A	RESERVED pin	Leave unconnected.
32	GND	GND	N/A	Ground	All GND pins must be connected to ground.
33	ETH_TX_CTL	ETH	O	Ethernet Transmit Control	RGMII: Control signal for the transmit data (TXEN on TXC rising edge; TXEN xor TXER on TXC falling edge). RMII: Control signal for the transmit data (TX_EN). See section 4.2.13 for detailed electrical specs.
34	ETH_TXD3	ETH	O	Ethernet Transmit Data [3]	RGMII: Tx data bit 3 / 7 on TXC rising / falling edges. RMII: Not used. See section 4.2.13 for detailed electrical specs.
35	ETH_TXD2	ETH	O	Ethernet Transmit Data [2]	RGMII: Tx data bit 2 / 6 on TXC rising / falling edges. RMII: Not used. See section 4.2.13 for detailed electrical specs.
36	ETH_TXD1	ETH	O	Ethernet Transmit Data [1]	RGMII: Tx data bit 1 / 5 on TXC rising / falling edges. RMII: Tx data bit 1 in sync with REF_CLK. See section 4.2.13 for detailed electrical specs.
37	ETH_TXD0	ETH	O	Ethernet Transmit Data [0]	RGMII: Tx data bit 0 / 4 on TXC rising / falling edges. RMII: Tx data bit 0 in sync with REF_CLK. See section 4.2.13 for detailed electrical specs.
38	ETH_RXD0	ETH	I	Ethernet Receive Data [0]	RGMII: Rx data bit 0 / 4 on RXC rising / falling edges. RMII: Rx data bit 0 in sync with REF_CLK. See section 4.2.13 for detailed electrical specs.
39	ETH_RXD1	ETH	I	Ethernet Receive Data [1]	RGMII: Rx data bit 1 / 5 on RXC rising / falling edges. RMII: Rx data bit 1 in sync with REF_CLK. See section 4.2.13 for detailed electrical specs.
40	ETH_RXD2	ETH	I	Ethernet Receive Data [2]	RGMII: Rx data bit 2 / 6 on RXC rising / falling edges. RMII: Not used. See section 4.2.13 for detailed electrical specs.
41	ETH_RXD3	ETH	I	Ethernet Receive Data [3]	RGMII: Rx data bit 3 / 7 on RXC rising / falling edges. RMII: Not used. See section 4.2.13 for detailed electrical specs.
42	ETH_RX_CTL	ETH	I	Ethernet Receive Control	RGMII: Control signal for receive data (RXDV on RXC rising edge; RXDV xor RXER on RXC falling edge). RMII: Control signal for receive data, contains carrier sense (CRS) and data valid (RX_DV) information. See section 4.2.13 for detailed electrical specs.
43	ETH_RX_CLK	ETH	I	Ethernet Receive Clock	RGMII: Receive reference clock (RXC). RMII: Not used. See section 4.2.13 for detailed electrical specs.
44	GND	GND	N/A	Ground	All GND pins must be connected to ground.

No	Name	Power domain	I/O	Description	Remarks
45	RSVD	-	N/A	RESERVED pin	Leave unconnected.
46	GND	GND	N/A	Ground	All GND pins must be connected to ground.
47	RSVD	-	N/A	RESERVED pin	Leave unconnected.
48	RSVD	-	N/A	RESERVED pin	Leave unconnected.
49	RSVD	-	N/A	RESERVED pin	Leave unconnected.
50	I2S_WA	GDI	I/O	I2S0 word alignment	I^2S word alignment. See section 4.2.15 for detailed electrical specs.
51	I2S_TXD	GDI	O	I2S0 transmit data	I^2S transmit data out. See section 4.2.15 for detailed electrical specs.
52	I2S_CLK	GDI	I/O	I2S0 clock	I^2S serial clock. See section 4.2.15 for detailed electrical specs.
53	I2S_RXD	GDI	I	I2S0 receive data	I^2S receive data. See section 4.2.15 for detailed electrical specs
54	SCL	DDC	O	I2C0 clock	I^2C bus serial clock line. Fixed open drain. No internal pull-up. See section 4.2.12 for detailed electrical specs.
55	SDA	DDC	I/O	I2C0 data	I^2C bus serial data line. Fixed open drain. No internal pull-up. See section 4.2.12 for detailed electrical specs.
56	SIM_CLK	SIM	O	SIM0 clock	See section 4.2.10 for detailed electrical specs.
57	SIM_IO	SIM	I/O	SIM0 data	Internal 4.7 kΩ pull-up resistor to VSIM. See section 4.2.10 for detailed electrical specs.
58	SIM_RST	SIM	O	SIM0 reset	See section 4.2.10 for detailed electrical specs.
59	VSIM	-	O	SIM0 supply output	VSIM = 1.8 V or 2.9 V generated by the module according to the external SIM card/chip voltage type. See section 4.2.3 for detailed electrical specs.
60	GPIO5	GDI	I/O	GPIO	GPIO configurable as described in section 2.9. See section 4.2.15 for detailed electrical specs.
61	GPIO6	GDI	I/O	GPIO	GPIO configurable as described in section 2.9. See section 4.2.15 for detailed electrical specs.
62	HOST_SELECT1	GDI	I / I/O	Input for selection of module setting by the host processor	Alternately settable as GPIO by uCPU API Alternately settable as External Interrupt by uCPU API See section 4.2.15 for detailed electrical specs.
63	SDIO_D2	GDI	I/O	SDIO serial data [2]	See section 4.2.15 for detailed electrical specs.
64	SDIO_CLK	GDI	O	SDIO serial clock	See section 4.2.15 for detailed electrical specs.
65	SDIO_CMD	GDI	I/O	SDIO command	See section 4.2.15 for detailed electrical specs.
66	SDIO_D0	GDI	I/O	SDIO serial data [0]	See section 4.2.15 for detailed electrical specs.
67	SDIO_D3	GDI	I/O	SDIO serial data [3]	See section 4.2.15 for detailed electrical specs.
68	SDIO_D1	GDI	I/O	SDIO serial data [1]	See section 4.2.15 for detailed electrical specs.
69	GND	GND	N/A	Ground	All GND pins must be connected to ground.
70	VCC	VCC	I	Module supply input	All VCC pins must be connected to external supply. See section 4.2.3 for detailed electrical specs.
71	VCC	VCC	I	Module supply input	All VCC pins must be connected to external supply. See section 4.2.3 for detailed electrical specs.
72	VCC	VCC	I	Module supply input	All VCC pins must be connected to external supply. See section 4.2.3 for detailed electrical specs.
73	GND	GND	N/A	Ground	All GND pins must be connected to ground.
74	GND	GND	N/A	Ground	All GND pins must be connected to ground.
75	ANT_DET	ADC	I	Antenna detection	Antenna presence detection function.
76	GND	GND	N/A	Ground	All GND pins must be connected to ground.
77	RSVD	-	N/A	RESERVED pin	Leave unconnected.
78	GND	GND	N/A	Ground	All GND pins must be connected to ground.
79	GND	GND	N/A	Ground	All GND pins must be connected to ground.
80	GND	GND	N/A	Ground	All GND pins must be connected to ground.

No	Name	Power domain	I/O	Description	Remarks
81	ANT1	ANT	I/O	Primary antenna	50 Ω nominal characteristic impedance. Main Tx / Rx antenna interface. See section 4.2.5 / 4.2.6 / 4.2.7 for details.
82	GND	GND	N/A	Ground	All GND pins must be connected to ground.
83	GND	GND	N/A	Ground	All GND pins must be connected to ground.
84	RSVD	-	N/A	RESERVED pin	Leave unconnected.
85	GND	GND	N/A	Ground	All GND pins must be connected to ground.
86	GND	GND	N/A	Ground	All GND pins must be connected to ground.
87	ANT2	ANT	I	Secondary antenna	50 Ω nominal characteristic impedance Rx only for Down-Link MIMO and Rx diversity. See section 4.2.5 / 4.2.6 / 4.2.7 for details.
88	GND	GND	N/A	Ground	All GND pins must be connected to ground.
89	GND	GND	N/A	Ground	All GND pins must be connected to ground.
90	GND	GND	N/A	Ground	All GND pins must be connected to ground.
91	RSVD	-	N/A	RESERVED pin	Leave unconnected.
92	GND	GND	N/A	Ground	All GND pins must be connected to ground.
93-152	GND	GND	N/A	Ground	All GND pins must be connected to ground.
153	RSVD	-	N/A	RESERVED pin	Leave unconnected.
154	RSVD	-	N/A	RESERVED pin	Leave unconnected.
155	RSVD	-	N/A	RESERVED pin	Leave unconnected.
156	RSVD	-	N/A	RESERVED pin	Leave unconnected.
157	RSVD	-	N/A	RESERVED pin	Leave unconnected.
158	RSVD	-	N/A	RESERVED pin	Leave unconnected.
159	TXD1	GDI	I / I	UART1 data input / SPI1 Master Input Slave Output	Circuit 103 (TxD) in ITU-T V.24. Alternatively configurable as SPI1 Master In Slave Out. See section 4.2.15 for detailed electrical specs.
160	RXD1	GDI	O / O	UART1 data output / SPI1 Master Output Slave Input	Circuit 104 (RxD) in ITU-T V.24. Alternatively configurable as SPI1 Master Out Slave In. See section 4.2.15 for detailed electrical specs.
161	TXD2	GDI	I	UART2 data input	Circuit 103 (TxD) in ITU-T V.24. See section 4.2.15 for detailed electrical specs.
162	RXD2	GDI	O	UART2 data output	Circuit 104 (RxD) in ITU-T V.24. See section 4.2.15 for detailed electrical specs.
163	RSVD	-	N/A	RESERVED pin	Leave unconnected.
164	RSVD	-	N/A	RESERVED pin	Leave unconnected.
165	RSVD	-	N/A	RESERVED pin	Leave unconnected.
166	RSVD	-	N/A	RESERVED pin	Leave unconnected.
167	RSVD	-	N/A	RESERVED pin	Leave unconnected.
168	USB_ID	USB2	I	USB device identification	Pin for USB ID resistance measurement.
169	SPI_MISO	GDI	I	SPI0 Master Input Slave Output	SPI0 data input See section 4.2.15 for detailed electrical specs.
170	USB_SSRX+	USB3	I	USB Super-Speed 3.0 differential receiver (+)	90 Ω nominal differential characteristic impedance Compliant with USB Revision 3.0 specification [13]. See section 4.2.11 for detailed electrical specs.
171	USB_SSRX–	USB3	I	USB Super-Speed 3.0 differential receiver (–)	90 Ω nominal differential characteristic impedance Compliant with USB Revision 3.0 specification [13]. See section 4.2.11 for detailed electrical specs.
172	VSIM1	-	O	SIM1 supply output	VSIM1 = 1.8 V or 2.9 V, generated by the module according to the external SIM card/chip voltage type. See section 4.2.3 for detailed electrical specs.
173	SPI_CS	GDI	O	SPI0 Chip Select 0	SPI0 chip select output See section 4.2.15 for detailed electrical specs.
174	SPI_MOSI	GDI	O	SPI0 Master Output Slave Input	SPI0 data output See section 4.2.15 for detailed electrical specs.

No	Name	Power domain	I/O	Description	Remarks
175	USB_SSTX+	USB3	O	USB Super-Speed 3.0 differential transmitter (+)	90 Ω nominal differential characteristic impedance. Internal series 100 nF capacitor for AC coupling. Compliant with USB Revision 3.0 specification [13]. See section 4.2.11 for detailed electrical specs.
176	USB_SSTX–	USB3	O	USB Super-Speed 3.0 differential transmitter (–)	90 Ω nominal differential characteristic impedance. Internal series 100 nF capacitor for AC coupling. Compliant with USB Revision 3.0 specification [13]. See section 4.2.11 for detailed electrical specs.
177	SIM1_RST	SIM	O	SIM1 reset	See section 4.2.10 for detailed electrical specs.
178	SIM1_IO	SIM	I/O	SIM1 data	Internal 4.7 kΩ pull-up resistor to VSIM1. See section 4.2.10 for detailed electrical specs.
179	SPI_SCLK	GDI	O	SPI0 Shift Clock	SPI0 clock output See section 4.2.15 for detailed electrical specs.
180	RSVD	-	N/A	RESERVED pin	Leave unconnected.
181	RSVD	-	N/A	RESERVED pin	Leave unconnected.
182	SIM1_CLK	SIM	O	SIM1 clock	See section 4.2.10 for detailed electrical specs.
183	RSVD	-	N/A	RESERVED pin	Leave unconnected.
184	RSVD	-	N/A	RESERVED pin	Leave unconnected.
185	RSVD	-	N/A	RESERVED pin	Leave unconnected.
186	RSVD	-	N/A	RESERVED pin	Leave unconnected.
187	RSVD	-	N/A	RESERVED pin	Leave unconnected.
188	RSVD	-	N/A	RESERVED pin	Leave unconnected.
189	RSVD	-	N/A	RESERVED pin	Leave unconnected.
190	RSVD	-	N/A	RESERVED pin	Leave unconnected.
191	RSVD	-	N/A	RESERVED pin	Leave unconnected.
192	RSVD	-	N/A	RESERVED pin	Leave unconnected.
193	RTS1	GDI	I / O	UART1 ready to send / SPI1 Shift Clock	Circuit 105 (RTS) in ITU-T V.24. Alternatively configurable as SPI1 Shift Clock. See section 4.2.15 for detailed electrical specs.
194	RSVD	-	N/A	RESERVED pin	Leave unconnected.
195	CTS1	GDI	O / O	UART1 clear to send / SPI1 Chip Select	Circuit 106 (CTS) in ITU-T V.24. Alternatively configurable as SPI1 Chip Select. See section 4.2.15 for detailed electrical specs.
196	RSVD	-	N/A	RESERVED pin	Leave unconnected.
197	RSVD	-	N/A	RESERVED pin	Leave unconnected.
198	RSVD	-	N/A	RESERVED pin	Leave unconnected.
199	RSVD	-	N/A	RESERVED pin	Leave unconnected.
200	RSVD	-	N/A	RESERVED pin	Leave unconnected.
201	RSVD	-	N/A	RESERVED pin	Leave unconnected.
202	RSVD	-	N/A	RESERVED pin	Leave unconnected.
203	SCL1	DDC	O	I2C1 clock	I^2C bus serial clock line. Fixed open drain. No internal pull-up. See section 4.2.12 for detailed electrical specs.
204	SDA1	DDC	I/O	I2C1 data	I^2C bus serial data line. Fixed open drain. No internal pull-up. See section 4.2.12 for detailed electrical specs.
205	I2S1_WA	GDI	I/O	I2S1 word alignment	I^2S word alignment. See section 4.2.15 for detailed electrical specs.
206	I2S1_TXD	GDI	O	I2S1 transmit data	I^2S transmit data out. See section 4.2.15 for detailed electrical specs.
207	I2S1_RXD	GDI	I	I2S1 receive data	I^2S receive data. See section 4.2.15 for detailed electrical specs.
208	I2S1_CLK	GDI	I/O	I2S1 clock	I^2S serial clock. See section 4.2.15 for detailed electrical specs

No	Name	Power domain	I/O	Description	Remarks
209	GND	GND	N/A	Ground	All GND pins must be connected to ground.
210	V_MMC	MMC	O	Multi-Media Card Interface supply output	1.80 V / 2.85 V (typical) output voltage generated by the module. See section 4.2.3 for detailed electrical specs.
211	MMC_RST_N	MMC	O	Multi-Media Card Reset	See section 4.2.14 for detailed electrical specs
212	MMC_D1	MMC	I/O	Multi-Media Card Data [1]	See section 4.2.14 for detailed electrical specs
213	MMC_D3	MMC	I/O	Multi-Media Card Data [3]	See section 4.2.14 for detailed electrical specs
214	MMC_D0	MMC	I/O	Multi-Media Card Data [0]	See section 4.2.14 for detailed electrical specs
215	MMC_CMD	MMC	I/O	Multi-Media Card Command	See section 4.2.14 for detailed electrical specs
216	MMC_CLK	MMC	I/O	Multi-Media Card Clock	See section 4.2.14 for detailed electrical specs
217	MMC_D2	MMC	I/O	Multi-Media Card Data [2]	See section 4.2.14 for detailed electrical specs
218	MMC_CD_N	MMC	I	Multi-Media Card Detect	See section 4.2.14 for detailed electrical specs
219	GND	GND	N/A	Ground	All GND pins must be connected to ground.
220	ETH_INTR	ETH	I	Ethernet Interrupt Input	When this signal is high, it indicates an interrupt event in the PHY. See section 4.2.13 for detailed electrical specs.
221	V_ETH	ETH	O	Ethernet Interface supply output	2.5 V / 3.3 V (typical) output voltage generated by the module when it is switched-on. See section 4.2.3 for detailed electrical specs.
222	ETH_MDIO	ETH	I/O	Ethernet Management Data Input Output	See section 4.2.13 for detailed electrical specs.
223	ETH_MDC	ETH	O	Ethernet Management Data Clock	See section 4.2.13 for detailed electrical specs.
224	RSVD	-	N/A	RESERVED pin	Leave unconnected.
225	RSVD	-	N/A	RESERVED pin	Leave unconnected.
226	GND	GND	N/A	Ground	All GND pins must be connected to ground.
227	SPK_P	AUDIO	O	Differential analog audio output (+)	See section 4.2.16 for detailed electrical specs.
228	SPK_N	AUDIO	O	Differential analog audio output (–)	See section 4.2.16 for detailed electrical specs.
229	GND	GND	N/A	Ground	All GND pins must be connected to ground.
230	MIC_GND	AUDIO	I	Microphone analog reference	Local ground for the external microphone. See section 4.2.16 for detailed electrical specs.
231	MIC_BIAS	AUDIO	O	Microphone supply output	See section 4.2.16 for detailed electrical specs.
232	GND	GND	N/A	Ground	All GND pins must be connected to ground.
233	MIC2_N	AUDIO	I	MIC2 differential analog audio input (–)	See section 4.2.16 for detailed electrical specs.
234	MIC2_P	AUDIO	I	MIC2 differential analog audio input (+)	See section 4.2.16 for detailed electrical specs.
235	GND	GND	N/A	Ground	All GND pins must be connected to ground.
236	MIC1_N	AUDIO	I	MIC1 differential analog audio input (–)	See section 4.2.16 for detailed electrical specs.
237	MIC2_P	AUDIO	I	MIC1 differential analog audio input (+)	See section 4.2.16 for detailed electrical specs.
238	GND	GND	N/A	Ground	All GND pins must be connected to ground.
239	ADC2	ADC	I	ADC input	See section 4.2.17 for detailed electrical specs.
240	ADC1	ADC	I	ADC input	See section 4.2.17 for detailed electrical specs.
241	GND	GND	N/A	Ground	All GND pins must be connected to ground.
242	RSVD	-	N/A	RESERVED pin	Leave unconnected.
243	RSVD	-	N/A	RESERVED pin	Leave unconnected.
244	RSVD	-	N/A	RESERVED pin	Leave unconnected.
245	RSVD	-	N/A	RESERVED pin	Leave unconnected.
246	RSVD	-	N/A	RESERVED pin	Leave unconnected.

No	Name	Power domain	I/O	Description	Remarks
247	GPIO8	GDI	I/O	GPIO	GPIO configurable as described in section 2.9. See section 4.2.15 for detailed electrical specs.
248	GPIO7	GDI	I/O	GPIO	GPIO configurable as described in section 2.9. See section 4.2.15 for detailed electrical specs.

Table 6: TOBY-L4 series pin-out

☞ For more information about the pin-out, see the TOBY-L4 series System Integration Manual [2].

☞ See Appendix A for an explanation of abbreviations and terms used.

4 Electrical specifications

Stressing the device above one or more of the ratings listed in the Absolute Maximum Rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating Conditions sections (section 4.2) of the specification should be avoided. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating condition ranges define those limits within which the functionality of the device is guaranteed.

Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum rating

Limiting values given below are in accordance with the Absolute Maximum Rating System (IEC 134).

Symbol	Description	Condition	Min.	Max.	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	–0.3	5.5	V
VUSB_DET	USB detection pin	Input DC voltage at VUSB_DET pin	–0.3	5.5	V
USB2	USB 2.0 pins	Input DC voltage at USB 2.0 interface pins	–0.3	3.6	V
DDC	DDC interface	Input DC voltage at DDC interface pins	–0.3	2.3	V
GDI	Generic digital interfaces	Input DC voltage at Generic digital interfaces pins	–0.3	2.3	V
SIM	SIM interface	Input DC voltage at SIM interface pins	–0.3	3.3	V
ERS	External reset signal	Input DC voltage at RESET_N pin	–0.3	2.3	V
POS	Power-on input	Input DC voltage at PWR_ON pin	–0.3	1.7	V
Tstg	Storage Temperature		–40	+95	°C

Table 7: Absolute maximum ratings

The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD

Parameter	Min	Typical	Max	Unit	Remarks
ESD sensitivity for all pins except ANT1 / ANT2 pins			1000	V	Human Body Model according to JESD22-A114
ESD sensitivity for ANT1 / ANT2 pins			1000	V	Human Body Model according to JESD22-A114

Table 8: Maximum ESD ratings

u-blox cellular modules are Electrostatic Sensitive Devices and require special precautions when handling. See section 7.4 for ESD handling instructions.

4.2 Operating conditions

Unless otherwise indicated, all operating condition specifications are at an ambient temperature of 25 °C.

Operation beyond the operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating temperature range

Parameter	Min.	Typical	Max.	Unit	Remarks
Normal operating temperature	–20	+25	+75	°C	Normal operating temperature range (fully functional and meet 3GPP specifications)
Extended operating temperature	–40		+85	°C	Extended operating temperature range (RF performance may be affected outside normal operating range, though the module is fully functional)
eCall operating temperature	–40		+95	°C	eCall operating temperature range (emergency call sustained for at least 2 minutes)

Table 9: Environmental conditions

4.2.2 Module thermal parameters

Symbol	Parameter	Min.	Typical	Max.	Unit	Remarks
$\theta_{J\text{-}B}$	Junction-to-Board thermal resistance		12.8		°C/W	Part of the Two-Resistor Compact Thermal Model of the module, defined according to JEDEC Standard No. 51 and/or JEDEC Standard No. 15
$\theta_{J\text{-}Ctop}$	Junction-to-Case thermal resistance		17.5		°C/W	Part of the Two-Resistor Compact Thermal Model of the module, defined according to JEDEC Standard No. 51 and/or JEDEC Standard No. 15

Table 10: Two-Resistor Compact Thermal Model of the TOBY-L4 series module

Symbol	Parameter	Min.	Typical	Max.	Unit	Remarks
$\theta_{J\text{-}A}$	Junction-to-Ambient thermal resistance		20.9		°C/W	Standardized thermal figure, defined according to JEDEC Standard No. 51

Table 11: Junction-to-Ambient thermal resistance of the TOBY-L4 series module

4.2.3 Supply/power pins

Symbol	Parameter	Min.	Typical	Max.	Unit
VCC	Module supply normal operating input voltage[12]	3.30	3.80	4.40	V
	Module supply extended operating input voltage[13]	3.00	3.80	4.50	V
V_BCKP	Real Time Clock supply input voltage	1.60		3.40	V
I_BCKP	Real Time Clock supply average current consumption, at V_BCKP = 2.5 V		2	5	µA

Table 12: Input characteristics of the Supply/Power pins

Symbol	Parameter	Min.	Typical	Max.	Unit
VSIM	SIM supply output voltage with external 1.8 V SIM		1.80		V
	SIM supply output voltage with external 3.0 V SIM		2.90		V
V_BCKP	Real Time Clock supply output voltage		2.50		V
I_BCKP	Real Time Clock supply output current capability			0.5	mA
V_INT	Generic Digital Interfaces supply output voltage		1.80		V
I_INT	Generic Digital Interfaces supply output current capability			70	mA

Table 13: Output characteristics of the Supply/Power pins

[12] Input voltage at **VCC** must be above the normal operating range minimum limit to switch-on the module. RF performance may be affected when the input voltage at **VCC** is outside the herein stated normal operating range limits, though the module is still fully functional when the input voltage at **VCC** is inside the extended operating range limits.

[13] Ensure that input voltage at **VCC** never drops below the extended operating range minimum limit during module operation: the cellular module may switch-off when the **VCC** voltage value drops below the herein stated extended operating range minimum limit.

4.2.4 Current consumption

Mode	Condition	Tx power	Min	Typ[14]	Max[15]	Unit
Power Off Mode	Average current with module switched off, VCC supply present			0.1		mA
Idle-Mode	Base current, equivalent to Airplane Mode, with Power Saving enabled and interfaces not used			2.4		mA
Cyclic Idle/Active-Mode	Average current in Discontinuous Reception, with Power Saving enabled and interfaces not used			3.9		mA
2G Connected Mode	Average current during 2G GMSK call	Minimum		0.12		A
	Average current during 2G GMSK call	Maximum		0.38		A
	Pulse current[16] during a 1-slot GMSK Tx burst	Maximum		1.90	2.50	A
3G Connected Mode	Average current during 3G call, with Low data rate	0 dBm		0.14		A
		Maximum		0.65		A
LTE Connected Mode	Average current during LTE call, with Low data rate	0 dBm		0.14		A
		Maximum		0.69		A
	Average current during LTE call, with Max data rate, Max CPU usage	Maximum		1.20	1.50	A

Table 14: Module VCC current consumption

[14] Typical values with a matched antenna.
[15] Maximum values with a mismatched antenna.
[16] It is recommended to use this figure to dimension maximum current capability of power supply.

4.2.5 LTE RF characteristics

The LTE bands supported by each TOBY-L4 series module are defined in Table 1, while Table 15 describes the Tx / Rx frequencies for each LTE band according to 3GPP TS 36.521-1 [9].

Parameter		Min.	Max.	Unit	Remarks
Frequency range FDD Band 12 (700 MHz)	Uplink	699	716	MHz	Module transmit
	Downlink	729	746	MHz	Module receive
Frequency range FDD Band 17 (700 MHz)	Uplink	704	716	MHz	Module transmit
	Downlink	734	746	MHz	Module receive
Frequency range FDD Band 29 (700 MHz)	Uplink	1850	1910	MHz	Module transmit (carrier aggregation using band 2)
	Downlink	717	728	MHz	Module receive
Frequency range FDD Band 28 (750 MHz)	Uplink	703	748	MHz	Module transmit
	Downlink	758	803	MHz	Module receive
Frequency range FDD Band 13 (750 MHz)	Uplink	777	787	MHz	Module transmit
	Downlink	746	756	MHz	Module receive
Frequency range FDD Band 20 (800 MHz)	Uplink	832	862	MHz	Module transmit
	Downlink	791	821	MHz	Module receive
Frequency range FDD Band 5 (850 MHz)	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range FDD Band 19 (850 MHz)	Uplink	830	845	MHz	Module transmit
	Downlink	875	890	MHz	Module receive
Frequency range FDD Band 8 (900 MHz)	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range FDD Band 4 (1700 MHz)	Uplink	1710	1755	MHz	Module transmit
	Downlink	2110	2155	MHz	Module receive
Frequency range FDD Band 3 (1800 MHz)	Uplink	1710	1785	MHz	Module transmit
	Downlink	1805	1880	MHz	Module receive
Frequency range FDD Band 9 (1800 MHz)	Uplink	1749.9	1784.9	MHz	Module transmit
	Downlink	1844.9	1879.9	MHz	Module receive
Frequency range FDD Band 2 (1900 MHz)	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range FDD Band 25 (1900 MHz)	Uplink	1850	1915	MHz	Module transmit
	Downlink	1930	1995	MHz	Module receive
Frequency range TDD Band 39 (1900 MHz)	Uplink	1880	1920	MHz	Module transmit
	Downlink	1880	1920	MHz	Module receive
Frequency range FDD Band 1 (2100 MHz)	Uplink	1920	1980	MHz	Module transmit
	Downlink	2110	2170	MHz	Module receive
Frequency range TDD Band 40 (2300 MHz)	Uplink	2300	2400	MHz	Module transmit
	Downlink	2300	2400	MHz	Module receive
Frequency range TDD Band 41 (2500 MHz)	Uplink	2555	2655	MHz	Module transmit
	Downlink	2555	2655	MHz	Module receive
Frequency range TDD Band 38 (2600 MHz)	Uplink	2570	2620	MHz	Module transmit
	Downlink	2570	2620	MHz	Module receive
Frequency range FDD Band 7 (2600 MHz)	Uplink	2500	2570	MHz	Module transmit
	Downlink	2620	2690	MHz	Module receive

Table 15: LTE operating RF frequency bands

TOBY-L4 series modules include an LTE-FDD / LTE-TDD Power Class 3 transmitter (see Table 2) and LTE-FDD / LTE-TDD receivers with RF characteristics according to 3GPP TS 36.521-1 [9].

Parameter	Min.	Typical	Max.	Unit	Remarks
Receiver input sensitivity Band 3 (1800 MHz)		–110.0		dBm	Channel bandwidth = 1.4 MHz
		–105.0		dBm	Channel bandwidth = 5 MHz
		–99.5		dBm	Channel bandwidth = 20 MHz
Receiver input sensitivity Band 39 (1900 MHz)		–105.5		dBm	Channel bandwidth = 5 MHz
		–100.0		dBm	Channel bandwidth = 20 MHz
Receiver input sensitivity Band 1 (2100 MHz)		–106.0		dBm	Channel bandwidth = 5 MHz
		–100.5		dBm	Channel bandwidth = 20 MHz
Receiver input sensitivity Band 40 (2300 MHz)		–105.5		dBm	Channel bandwidth = 5 MHz
		–100.0		dBm	Channel bandwidth = 20 MHz
Receiver input sensitivity Band 41 (2500 MHz)		–104.5		dBm	Channel bandwidth = 5 MHz
		–98.5		dBm	Channel bandwidth = 20 MHz
Condition: 50 Ω source, Throughput > 95%, dual receiver, QPSK modulation, Other settings as per 3GPP TS 36.521-1 [9]					

Table 16: LTE receiver sensitivity performance

4.2.6 3G RF characteristics

The 3G bands supported by each TOBY-L4 series module are defined in Table 1, while Table 17 describes the Tx / Rx frequencies for each 3G band compliant with 3GPP TS 34.121-1 [10].

Parameter		Min.	Max.	Unit	Remarks
Frequency range UMTS FDD Band 5 (850 MHz)	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range UMTS FDD Band 8 (900 MHz)	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range UMTS FDD Band 4 (AWS, 1700 MHz)	Uplink	1710	1755	MHz	Module transmit
	Downlink	2110	2155	MHz	Module receive
Frequency range UMTS FDD Band 2 (1900 MHz)	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS FDD Band 1 (2100 MHz)	Uplink	1920	1980	MHz	Module transmit
	Downlink	2110	2170	MHz	Module receive

Table 17: 3G operating RF frequency bands

TOBY-L4 series modules include a W-CDMA (FDD) Power Class 3 transmitter (see Table 2) and receivers with RF characteristics compliant with 3GPP TS 34.121-1 [10].

Parameter	Min.	Typical	Max.	Unit	Remarks
Receiver input sensitivity Band 8 (900 MHz)		–111.5		dBm	Downlink RF level for RMC @ BER < 0.1%
Receiver input sensitivity Band 1 (2100 MHz)		–110.5		dBm	Downlink RF level for RMC @ BER < 0.1%
Condition: 50 Ω source, other settings as per 3GPP TS 34.121-1 [10]					

Table 18: 3G receiver sensitivity performance

4.2.7 2G RF characteristics

The 2G bands supported by each TOBY-L4 series module are defined in Table 1, while Table 19 describes the Tx / Rx frequencies for each 2G band according to 3GPP TS 51.010-1 [11].

Parameter		Min.	Max.	Unit	Remarks
Frequency range GSM 850	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range E-GSM 900	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range DCS 1800	Uplink	1710	1785	MHz	Module transmit
	Downlink	1805	1880	MHz	Module receive
Frequency range PCS 1900	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive

Table 19: 2G operating RF frequency bands

TOBY-L4 series modules include a GMSK Power Class 4 transmitter for GSM/E-GSM bands, a GMSK Power Class 1 transmitter for DCS/PCS bands, an 8-PSK Power Class E2 transmitter for all 2G bands (see Table 2), and related 2G receivers with RF characteristics compliant with 3GPP TS 51.010-1 [11].

Parameter	Min.	Typical	Max.	Unit	Remarks
Receiver input sensitivity E-GSM 900		–110.0		dBm	Downlink RF level @ BER Class II < 2.4%
Receiver input sensitivity DCS 1800		–109.0		dBm	Downlink RF level @ BER Class II < 2.4%

Condition: 50 Ω source, other settings as per 3GPP TS 51.010-1 [11]

Table 20: 2G receiver sensitivity performance

4.2.8 PWR_ON pin

Pin Name	Parameter	Min.	Typical	Max.	Unit	Remarks
PWR_ON	Internal supply for Power-On Input Signal		1.3		V	Internal 1.3 V supply rail
	Low-level input	–0.3		0.45	V	
	High-level input	0.85		1.6	V	
	Pull-up resistance		35		kΩ	Internal pull-up to 1.3 V supply rail
	PWR_ON low time	35		250	ms	Module switch-on
	PWR_ON low time	500		1000	ms	Module normal switch-off
	PWR_ON low time	2000			ms	Module emergency switch-off

Table 21: PWR_ON pin characteristics

4.2.9 RESET_N pin

Pin Name	Parameter	Min.	Typical	Max.	Unit	Remarks
RESET_N	Internal supply for External Reset Input Signal		1.8		V	Digital I/O Interfaces supply (V_INT)
	Low-level input			0.6	V	
	High-level input	1.2			V	
	Pull-up resistance		100		kΩ	Internal pull-up to V_INT
	RESET_N low time	50			ms	Low time to reset the module

Table 22: RESET_N pin characteristics

4.2.10 SIM pins

SIM pins are dedicated for connecting external SIM cards/chips. The electrical characteristics fulfill the regulatory specification requirements. The values in Table 23 are for information only.

Parameter	Min.	Typical	Max.	Unit	Remarks
Low-level input	–0.30		0.36	V	SIM supply = 1.8 V
	–0.30		0.58	V	SIM supply = 2.9 V
High-level input	1.26		2.10	V	SIM supply = 1.8 V
	2.03		3.20	V	SIM supply = 2.9 V
Low-level output		0.00	0.36	V	SIM supply = 1.8 V, Max value at I_{OL} = +1.0 mA
		0.00	0.58	V	SIM supply = 2.9 V, Max value at I_{OL} = +1.0 mA
High-level output	1.26	1.80		V	SIM supply = 1.8 V, Max value at I_{OL} = +1.0 mA
	2.03	2.90		V	SIM supply = 2.9 V, Max value at I_{OL} = +1.0 mA
Input / Output leakage current			0.7	µA	0.2V < V_{IN} < 3.2V
Clock frequency on SIM clock		3.9		MHz	
Internal pull-up resistor on SIM data		4.7		kΩ	Internal pull-up to SIM supply

Table 23: SIM pins characteristics

4.2.11 USB pins

USB Super-Speed 3.0 differential transmitter data lines (**USB_SSTX+** / **USB_SSTX**–) and USB Super-Speed 3.0 differential receiver data lines (**USB_SSRX+** / **USB_SSRX**–) comply with the USB Revision 3.0 specification [13]. The values in Table 24 are for information only.

Parameter	Min.	Typical	Max.	Unit	Remarks
Baud rate		5		Gbit/s	
Transmitter differential peak-to-peak voltage		1.0		V	
Transmitter de-emphasis		3.5		dB	
Transmitter differential characteristic impedance		90		Ω	
Receiver differential peak-to-peak voltage			1.2	V	
Receiver differential sensitivity	0.1			V	
Receiver differential characteristic impedance		90		Ω	

Table 24: USB Super-Speed 3.0 pin characteristics

USB High-Speed 2.0 differential transceiver data lines (**USB_D+** / **USB_D–**) are compliant with the Universal Serial Bus Revision 2.0 specification [14]. The values in Table 25 are for information only.

Parameter	Min.	Typical	Max.	Unit	Remarks
Baud rate		480		Mbit/s	
High-speed squelch detection threshold (input differential signal amplitude)	100		150	mV	
High speed disconnect detection threshold (input differential signal amplitude)	525		625	mV	
High-speed data signaling input common mode voltage range	–50		500	mV	
High-speed idle output level	–10		10	mV	
High-speed data signaling output high level	360		440	mV	
High-speed data signaling output low level	–10		10	mV	

Table 25: USB High-Speed 2.0 pins characteristics

The **VUSB_DET** input pin for the VBUS USB supply sense is compliant with USB Revision 3.0 specification [13] and USB Revision 2.0 specification [14]. The values in Table 26 are for information only.

Parameter	Min.	Typical	Max.	Unit	Remarks
VUSB_DET pin, High-level input	4.40	5.00	5.25	V	

Table 26: VUSB_DET pin characteristics

4.2.12 DDC (I²C) pins

The DDC (I²C) lines are compliant to the I²C-bus standard mode specification. See the I²C-Bus Specification [15] for detailed electrical characteristics. The values in Table 27 are for information only.

Parameter	Min	Typical	Max	Unit	Remarks
Internal supply for DDC domain		1.80		V	Digital I/O Interfaces supply (V_INT)
Low-level input	–0.30		0.54	V	
High-level input	1.26		2.00	V	
Low-level output		0.00	0.36	V	Max value at I_{OL} = +3.0 mA
Clock frequency		100		kHz	

Table 27: DDC (I²C) pin characteristics

4.2.13 RGMII pins

The Reduced Gigabit Media-Independent Interface complies with the RGMII Version 1.3 specification [16]. The values in Table 28 are for information only.

Parameter	Min	Typical	Max	Unit	Remarks
Internal supply for ETH domain		2.50		V	RGMII interface supply (V_ETH)
		3.30		V	RGMII interface supply (V_ETH)
Low-level input	–0.30		0.70	V	2.5 V mode
	–0.30		0.80	V	3.3 V mode
High-level input	1.70		2.80	V	2.5 V mode
	2.60		3.60	V	3.3 V mode
Low-level output		0.00		V	2.5 V mode
		0.00		V	3.3 V mode
High-level output		2.50		V	2.5 V mode
		3.30		V	3.3 V mode
Input / Output leakage current			10	µA	Pad in tri-state

Table 28: ETH pin characteristics

4.2.14 eMMC pins

The embedded Multi-Media Card interface complies with the JESD84-B451 Embedded Multimedia Card (eMMC) Electrical Standard 4.51 [17]. The values in Table 29 are for information only.

Parameter	Min	Typical	Max	Unit	Remarks
Internal supply for MMC domain		1.80		V	eMMC interface supply (V_MMC)
		2.85		V	eMMC interface supply (V_MMC)
Low-level input	–0.30		0.63	V	V_MMC = 1.80 V
	–0.30		0.71	V	V_MMC = 2.85V
High-level input	1.17		2.10	V	V_MMC = 1.80 V
	1.78		3.15	V	V_MMC = 2.85V
Low-level output		0.00		V	V_MMC = 1.80 V
		0.00		V	V_MMC = 2.85V
High-level output		1.80		V	V_MMC = 1.80 V
		2.85		V	V_MMC = 2.85V
Input / Output leakage current			0.7	µA	$0.2V < V_{IN} < 2.0V$

Table 29: MMC pin characteristics

4.2.15 Generic Digital Interfaces pins

Parameter	Min	Typical	Max	Unit	Remarks
Internal supply for GDI domain		1.80		V	Digital I/O Interfaces supply (V_INT)
Low-level input	–0.20		0.36	V	
High-level input	1.26		2.00	V	
Low-level output		0.00		V	
High-level output		1.80		V	
Input / Output leakage current			0.7	µA	$0.2V < V_{IN} < 2.0V$

Table 30: GDI pin characteristics

4.2.16 Analog audio pins

Parameter	Min	Typical	Max	Unit	Remarks
Microphone supply output voltage		2.2		V	Provided by MIC_BIAS output pin
Microphone supply output current			4.0	mA	Provided by MIC_BIAS output pin
Load capacitance			680	pF	Proper internal bypass capacitor already provided to guarantee stable operations: external capacitor directly connected to MIC_BIAS pin not required, but can be provided after a proper series resistor.
Load resistance	1			kΩ	
Microphone ground		0		V	MIC_GND pin is internally connected to ground as a sense line

Table 31: Microphone analog supply output (MIC_BIAS/MIC_GND) characteristics

Parameter	Min	Typical	Max	Unit	Remarks
Differential input voltage			1.6	Vpp	Full scale differential voltage
Differential input resistance		25		kΩ	
Common mode DC voltage		0.5		V	No internal DC blocking capacitor
Input capacitance		5	10	pF	No internal DC blocking capacitor
Dynamic range	72			dB FS CCIR-RMS	Gain stage = 0 dB, Bandwidth 300-8000 Hz, Input signal 0.8 Vpp differential
Total Harmonic Distortion plus Noise (THD+N)	–55			dB	Reference signal –10 dB FS
Power supply rejection	45	66		dB	

Table 32: Differential analog audio transmit paths input (MIC1_P/MIC1_N and MIC2_P/MIC2_N) characteristics

Parameter	Min	Typical	Max	Unit	Remarks
Maximum differential output voltage	3.3	3.7	4.1	Vpp	Full scale differential open circuit voltage
Common mode output voltage		1.25		V	No internal DC blocking capacitor
Output power			50	mW	Load = 16…32 Ω
Output current limit			200	mA	
Output load resistance	14			Ω	
Output load capacitance			250	pF	Between output pins and GND
Dynamic range	75	80		dB FS CCIR-RMS	Load = 16 Ω, Gain stage = +6 dB
Total Harmonic Distortion plus Noise (THD+N)	–50	–60		dB	Load = 16 Ω, Gain stage = +6 dB, Reference signal –10 dB FS

Table 33: Differential analog audio receive path output (SPK_P, SPK_N) characteristics

4.2.17 ADC pins

Parameter	Min.	Typ.	Max.	Unit	Remarks
Resolution		12		Bits	
Input voltage range	0		1.2	V	
Input resistance		102		kΩ	With respect to GND

Table 34: Analog to Digital Converter input pin (ADC1, ADC2) characteristics

5 Mechanical specifications

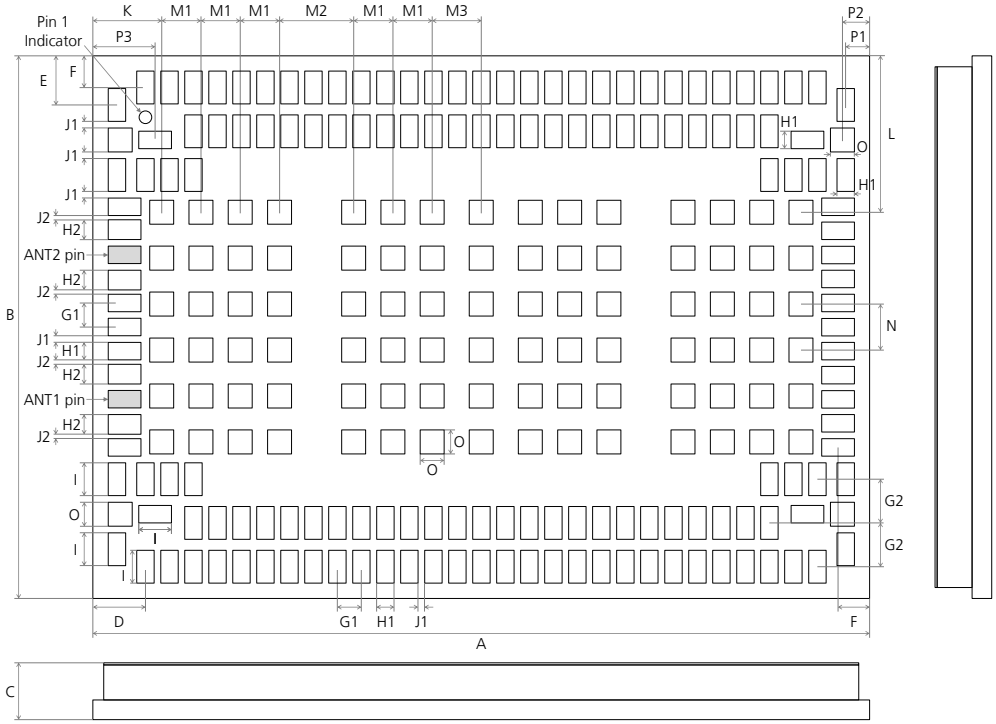


Figure 4: TOBY-L4 series dimensions (bottom and side views)

Parameter	Description	Typical		Tolerance	
A	Module Height [mm]	35.6	(1401.6 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
B	Module Width [mm]	24.8	(976.4 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
C	Module Thickness [mm]	2.6	(102.4 mil)	+0.27/–0.17	(+10.6/–6.7 mil)
D	Horizontal Edge to Lateral Pin Pitch [mm]	2.4	(94.5 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
E	Vertical Edge to Lateral Pin Pitch [mm]	2.25	(88.6 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
F	Edge to Lateral Pin Pitch [mm]	1.45	(57.1 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
G1	Lateral Pin to Pin Pitch [mm]	1.1	(43.3 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
G2	Lateral Pin to Pin Pitch [mm]	2.0	(78.7 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
H1	Lateral Pin Height [mm]	0.8	(31.5 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
H2	Lateral Pin close to ANT1 and ANT2 Height [mm]	0.9	(35.4 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
I	Lateral Pin Width [mm]	1.5	(59.1 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
J1	Lateral Pin to Pin Distance [mm]	0.3	(11.8 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
J2	Lateral Pin to Pin close to ANT Distance [mm]	0.2	(7.9 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
K	Horizontal Edge to Central Pin Pitch [mm]	3.15	(124.0 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
L	Vertical Edge to Central Pin Pitch [mm]	7.15	(281.5 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
M1	Central Pin to Pin Horizontal Pitch [mm]	1.8	(70.9 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
M2	Central Pin to Pin Horizontal Pitch [mm]	3.4	(133.9 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
M3	Central Pin to Pin Horizontal Pitch [mm]	2.25	(88.6 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
N	Central Pin to Pin Vertical Pitch [mm]	2.1	(82.7 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
O	Central Pin Height and Width [mm]	1.1	(43.3 mil)	+0.02/–0.02	(+0.8/–0.8 mil)
P1	Horizontal Edge to Corner Pin Pitch [mm]	1.1	(43.3 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
P2	Horizontal Edge to Corner Pin Pitch [mm]	1.25	(49.2 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
P3	Horizontal Edge to Corner Pin Pitch [mm]	2.85	(112.2 mil)	+0.20/–0.20	(+7.9/–7.9 mil)
Weight	Module Weight [g]	4.8			

Table 35: TOBY-L4 series dimensions

The module height tolerance +/– 0.20 mm may be exceeded close to the corners of the PCB due to cutting process: in worst case the height could be + 0.40 mm longer than the typical value.

6 Qualification and approvals

6.1 Reliability tests

Tests for product family qualifications according to ISO 16750 “Road vehicles - Environmental conditions and testing for electrical and electronic equipment“, and appropriate standards.

Extended qualification for automotive grade products.

6.2 Approvals

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

TOBY-L4 series modules are RoHS compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

Table 36 summarizes the main certification approvals for TOBY-L4 series modules.

Certification Scheme	TOBY-L4006	TOBY-L4106	TOBY-L4206	TOBY-L4906
GCF (Global Certification Forum)		•	•	•
PTCRB (PCS Type Certification Review Board)	•			
CE (Conformité Européenne)		•	•	•
FCC (US Federal Communications Commission)	•			
ISED (Innovation, Science & Economic Development Canada)[17]	•			
Anatel (Brazilian Certification)			•	
CCC (China Compulsory Certification)				•
SRRC (State Radio Regulation of China)				•
AT&T (US network operator)	•			

Table 36: TOBY-L4 series main certification approvals summary

For the complete list of approvals and for specific details on all country and network operators’ certifications, see our website www.u-blox.com or please contact the u-blox office or sales representative nearest you.

[17] Formerly known as IC (Industry Canada)

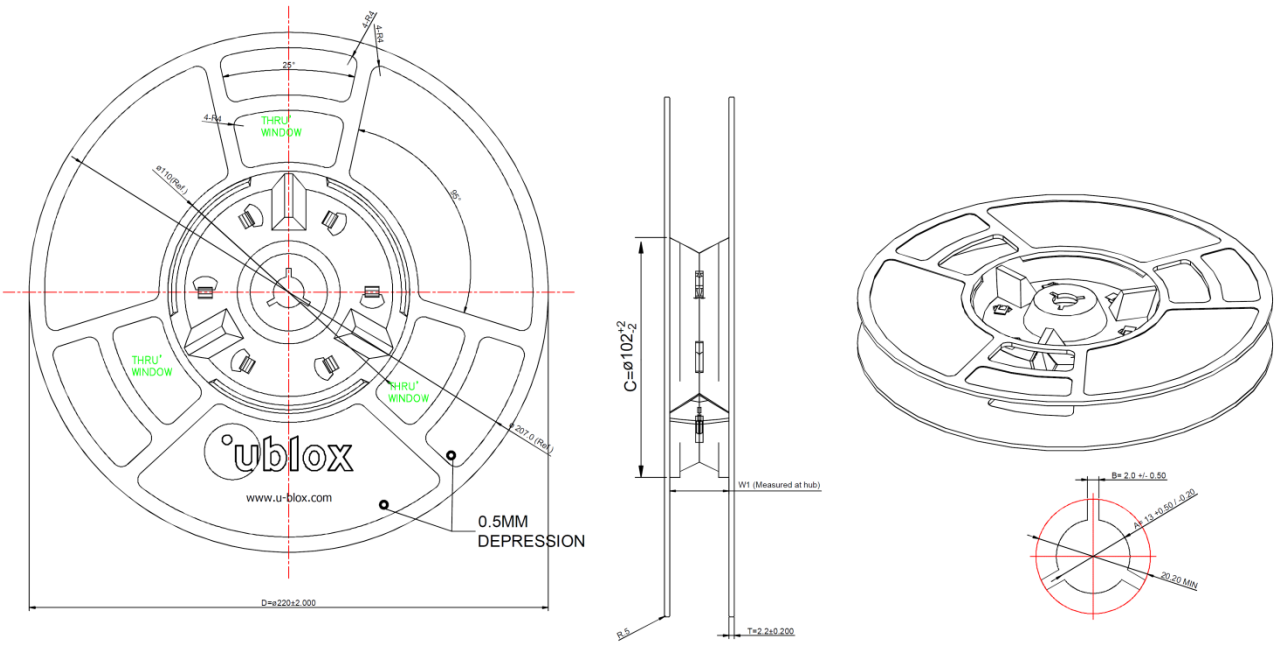
7 Product handling & soldering

7.1 Packaging

TOBY-L4 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox Package Information Guide [6].

7.1.1 Reels

TOBY-L4 series modules are deliverable in quantities of 150 pieces on a reel. The modules are delivered on the reel described in the Figure 5.



Tape Size (mm)	Flange Combination	Norminal Hub Width	W1
56	C9F2+C9F2 (28.5mm+28.5mm)	57mm	57 +0.5/-0.0 mm

Figure 5: TOBY-L4 series modules reel

Parameter	Specification
Reel Type	Described in Figure 5 above
Delivery Quantity	150

Table 37: Reel information for TOBY-L4 series modules

Quantities of less than 150 pieces are also available. Contact u-blox for more information.

7.1.2 Tapes

Figure 6 specifies the TOBY-L4 series modules' reeled tape dimensions.

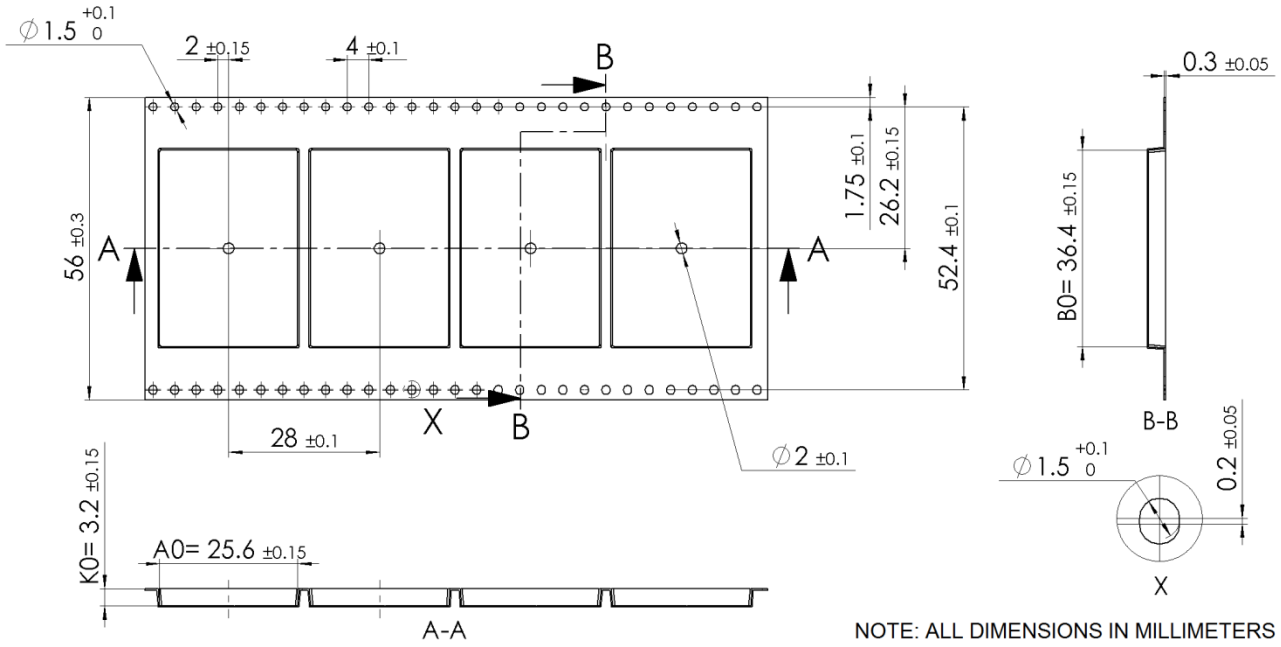


Figure 6: TOBY-L4 series modules tape

7.2 Moisture Sensitivity Levels

TOBY-L4 series modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. TOBY-L4 series modules are rated at MSL level 3. For more information regarding moisture sensitivity levels, labeling, storage and drying, see the u-blox Package Information Guide [6].

For the MSL standard, see IPC/JEDEC J-STD-020 (can be downloaded from www.jedec.org).

7.3 Reflow soldering

Reflow profiles are to be selected according to u-blox recommendations (see TOBY-L4 series System Integration Manual [2]).

Failure to observe these recommendations can result in severe damage to the device!

7.4 ESD precautions

TOBY-L4 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling TOBY-L4 series modules without proper ESD protection may destroy or damage them permanently.

TOBY-L4 series modules are Electrostatic Sensitive Devices (ESD) and require special ESD precautions as typically applied to ESD sensitive components.

Table 8 reports the maximum ESD ratings of the TOBY-L4 series modules.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates a TOBY-L4 series module.

ESD precautions should be implemented on the application board where the module is mounted, as described in the TOBY-L4 series System Integration Manual [2].

Failure to observe these recommendations can result in severe damage to the device!

8 Labeling and ordering information

8.1 Product labeling

The labels of TOBY-L4 series modules include important product information as described in this section.

Figure 7 illustrates the label of all the TOBY-L4 series modules, and includes: u-blox logo, production lot, lead-free marking, product type number, IMEI number, certifications identification numbers, CE marking (if applicable), and the production country.

Figure 7: TOBY-L4 series module label

8.2 Explanation of codes

Three different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all the u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 38 details these 3 different formats:

Format	Structure
Product Name	PPP(P)-TGVV(V)
Ordering Code	PPP(P)-TGVV(V)-MMQ
Type Number	PPP(P)-TGVV(V)-MMQ-XX

Table 38: Product code formats

Table 39 explains the parts of the product code.

Code	Meaning	Example
PPP(P)	Form factor	TOBY
TG	Platform (Technology and Generation) • Dominant technology: G: GSM; U: HSUPA; C: CDMA 1xRTT; N: NB-IoT; R: LTE low data rate (Cat 1 and below); L: LTE high data rate (Cat 3 and above) • Generation: 1…9	L4
VV(V)	Variant function set based on the same platform [00(0)…99(9)]	006
MM	Major product version [00…99]	00
Q	Product grade • B = professional • A = automotive	A
XX	Minor product version (not relevant for certification)	Default value is 00

Table 39: Part identification code

8.3 Ordering information

Ordering No.	Product
TOBY-L4006-00A	LTE Cat 6 module supporting LTE FDD / UMTS FDD / GSM, and u-blox uCPU for OEM applications Mainly designed for operation in North America, Automotive grade, 35.6 x 24.8 x 2.6 mm, 150 pcs/reel
TOBY-L4006-50A	LTE Cat 6 module supporting LTE FDD / UMTS FDD / GSM, and AT commands Mainly designed for operation in North America Automotive grade, 35.6 x 24.8 x 2.6 mm, 150 pcs/reel
TOBY-L4106-00A	LTE Cat 6 module supporting LTE FDD / LTE TDD / UMTS FDD / GSM, and u-blox uCPU for OEM applications Mainly designed for operation in EMEA Automotive grade, 35.6 x 24.8 x 2.6 mm, 150 pcs/reel
TOBY-L4106-50A	LTE Cat 6 module supporting LTE FDD / LTE TDD / UMTS FDD / GSM, and AT commands Mainly designed for operation in EMEA Automotive grade, 35.6 x 24.8 x 2.6 mm, 150 pcs/reel
TOBY-L4206-00A	LTE Cat 6 module supporting LTE FDD / UMTS FDD / GSM, and u-blox uCPU for OEM applications Mainly designed for operation in APAC / South America Automotive grade, 35.6 x 24.8 x 2.6 mm, 150 pcs/reel
TOBY-L4206-50A	LTE Cat 6 module supporting LTE FDD / UMTS FDD / GSM, and AT commands Mainly designed for operation in APAC / South America Automotive grade, 35.6 x 24.8 x 2.6 mm, 150 pcs/reel
TOBY-L4906-00A	LTE Cat 6 module supporting LTE FDD / LTE TDD / UMTS FDD / GSM, and u-blox uCPU for OEM applications Mainly designed for operation in China Automotive grade, 35.6 x 24.8 x 2.6 mm, 150 pcs/reel
TOBY-L4906-50A	LTE Cat 6 module supporting LTE FDD / LTE TDD / UMTS FDD / GSM, and AT commands Mainly designed for operation in China Automotive grade, 35.6 x 24.8 x 2.6 mm, 150 pcs/reel

Table 40: Product ordering codes

Appendix

A Glossary

Name	Definition
16QAM	16 Quadrature Amplitude Modulation
8-PSK	8 Phase-Shift Keying modulation
ACM	Abstract Control Model
ADC	Analog to Digital Converter
API	Application Program Interface
BER	Bit Error Rate
BSP	Board Support Package
CA	Carrier Aggregation
CDC	Communications Device Class
CSFB	Circuit Switched Fall-Back
DDC	Display Data Channel (I^2C compatible) Interface
DL	Down-link (Reception)
DRX	Discontinuous Reception
ECM	Ethernet networking Control Model
EDGE	Enhanced Data rates for GSM Evolution
eMMC	Embedded Multi-Media Card
ERS	External Reset Input Signal
ESD	Electrostatic Discharge
ETH	Ethernet RGMII / RMII interface (power domain)
FDD	Frequency Division Duplex
FOAT	Firmware update Over AT commands
FOTA	Firmware update Over The Air
FW	Firmware
GDI	Generic Digital Interfaces (power domain)
GMSK	Gaussian Minimum-Shift Keying modulation
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPS	Global Positioning System
GSM	Global System for Mobile Communication
H	High
HSDPA	High Speed Downlink Packet Access
HSM	Hardware Security Module
HSUPA	High Speed Uplink Packet Access
I	Input (means that this is an input port of the module)
I^2C	Inter-Integrated Circuit Interface
I^2S	Inter-IC Sound Interface
IMEI	International Mobile Equipment Identity
IMS	IP Multimedia Subsystem
L	Low
LGA	Land Grid Array
LTE	Long Term Evolution
MBIM	Mobile Broadband Interface Model
MIMO	Multi-Input Multi-Output

Name	Definition
MMC	Embedded Multi-Media Card / SD memory interface (power domain)
N/A	Not Applicable
NCM	Network Control Model
O	Output (means that this is an output port of the module)
OD	Open Drain
OEM	Original Equipment Manufacturer (company integrating a u-blox product)
PCN / IN	Product Change Notification / Information Note
PD	Pull-Down
POS	Power-On Input Signal
PU	Pull-Up
QPSK	Quadrature Phase-Shift Keying modulation
RGMII	Reduced Gigabit Media Independent Interface
RIL	Radio Interface Layer
RMC	Reference Measurement Channel
RMII	Reduced Media Independent Interface
RNDIS	Remote Network Driver Interface Specification
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDR	Single Data Rate
SHA	Secure Hash Algorithm
SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface
T	Tristate
TBD	To Be Defined
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver-Transmitter serial interface
uCPU	u-blox universal Central Processing Unit
UL	Up-link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
VM	Virtual Machine
VoLTE	Voice over LTE
W-CDMA	Wideband Code Division Multiple Access

Table 41: Explanation of abbreviations and terms used

Related documents

[1] u-blox AT Commands Manual, Docu No UBX-13002752

[2] u-blox TOBY-L4 series System Integration Manual, Docu No UBX-16024839

[3] u-blox TOBY-L4 series SDK Application Note, Docu No UBX-16022027

[4] u-blox TOBY-L4 series uCPU Build System Application Note, Docu No UBX-17001102

[5] u-blox TOBY-L4 series uCPU Platform Software Architecture Application Note, Docu No UBX-17001239

[6] u-blox Package Information Guide, Docu No UBX-14001652

[7] 3GPP TS 27.007 - AT command set for User Equipment (UE)

[8] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

[9] 3GPP TS 36.521-1 - Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; Part 1: Conformance Testing

[10] 3GPP TS 34.121-1 - User Equipment conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification

[11] 3GPP TS 51.010-1 - Mobile Station conformance specification; Part 1: Conformance specification

[12] ITU-T Recommendation V24, 02-2000. List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Connection Equipment (DCE)

[13] Universal Serial Bus Revision 3.0 specification, http://www.usb.org/developers/docs/documents_archive/

[14] Universal Serial Bus Revision 2.0 specification, http://www.usb.org/developers/docs/usb20_docs/

[15] I^2C-bus specification and user manual - Rev. 5 - 9 October 2012 - NXP Semiconductors, http://www.nxp.com/documents/user_manual/UM10204.pdf

[16] Reduced Gigabit Media-Independent Interface (RGMII) Version 1.3, www.hp.com/rnd/pdfs/RGMIIv1_3.pdf

[17] RMII Specification, Rev. 1.2

[18] JESD84-B451 - Embedded Multimedia Card (eMMC), Electrical Standard 4.51

For regular updates to u-blox documentation and to receive product change notifications, please register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	27-Apr-2016	sses / smoi	Initial release
R02	07-Oct-2016	sses	Remarked supported radio access technologies: LTE-FDD, LTE-TDD, UMTS FDD, (E)GPRS. Updated temperature range: Normal operating range –20 °C ÷ +75 °C, Extended operating range –40 °C ÷ +85 °C, eCall operating range –40 °C ÷ +95 °C Added UMTS band 8 on TOBY-L4906. Added I2S1 and UART3 interfaces. Added USB_ID pin. Updated RGMII / RMII interface electrical characteristics. Remarked Moisture Sensitivity Level: MSL 3. Added remark in mechanical description. Other minor corrections.
R03	13-Dec-2016	sses	Added GPIO, External Interrupt and SPI Chip Select functions support by specific pins. Other minor corrections.
R04	28-Jul-2017	sses	Added document applicability to "50" product versions. Updated FW features supported by "00" product versions. Updated 3G and 2G maximum data rate. Updated supported LTE CA. Updated LTE TDD Band 41 Frequency range. Clarified Rx diversity support. Updated Power-on, Power-off sections and PWR_ON pin specifications. Updated USB and UART supported functions / features. Updated SPI supported frequency. Clarified I2C and SDIO supported functions. Updated GPIOs supported functions. Renamed pin 230 from GND to MIC_GND. Updated support of digital audio interfaces. Added some Absolute maximum ratings, Module thermal parameters, Module VCC current consumption, Receivers sensitivity performances, and V_INT current capability. Updated main certification approvals. Minor other corrections.
R05	21-Nov-2017	sses	Added data rate supported by UART, SPI, I2C, SDIO interfaces Added USB capabilities Added GPIOs capabilities Added V_BCKP characteristics

Contact

For complete contact information, visit us at www.u-blox.com

u-blox Offices

North, Central and South America

u-blox America, Inc.
Phone: +1 703 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:
Phone: +1 408 573 3640
E-mail: info_us@u-blox.com

Technical Support:
Phone: +1 703 483 3185
E-mail: support_us@u-blox.com

Headquarters
Europe, Middle East, Africa

u-blox AG
Phone: +41 44 722 74 44
E-mail: info@u-blox.com
Support: support@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.
Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office Australia:
Phone: +61 2 8448 2016
E-mail: info_anz@u-blox.com
Support: support_ap@u-blox.com

Regional Office China (Beijing):
Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Chongqing):
Phone: +86 23 6815 1588
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shanghai):
Phone: +86 21 6090 4832
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shenzhen):
Phone: +86 755 8627 1083
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office India:
Phone: +91 80 4050 9200
E-mail: info_in@u-blox.com
Support: support_in@u-blox.com

Regional Office Japan (Osaka):
Phone: +81 6 6941 3660
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Japan (Tokyo):
Phone: +81 3 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:
Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:
Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com